74AHC595; 74AHCT595

8-bit serial-in/serial-out or parallel-out shift register with output latches

Rev. 6 — 26 May 2020 Product data sheet

1. General description

The 74AHC595; 74AHCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. The 74AHCT595 features TTL compatible inputs. Both 74AHC595 and 74AHCT595 inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Input levels:
  - The 74AHC595 operates with CMOS input levels
  - The 74AHCT595 operates with TTL input levels
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

nexperia

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC595D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT595D				
74AHC595PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT595PW				
74AHC595BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AHCT595BQ				

5. Functional diagram

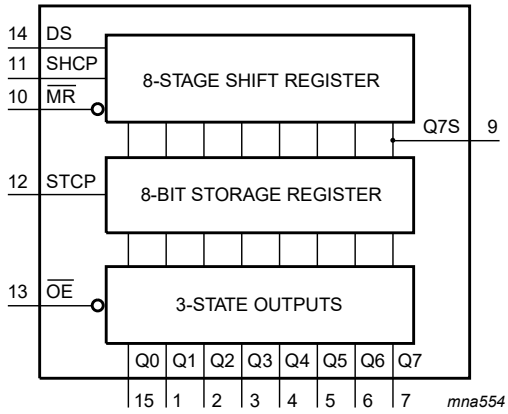


Fig. 1. Functional diagram

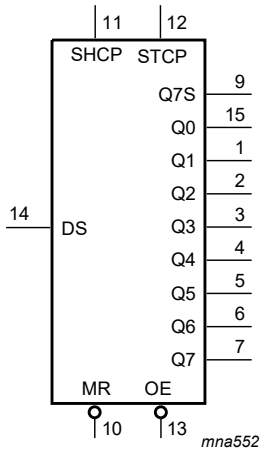


Fig. 2. Logic symbol

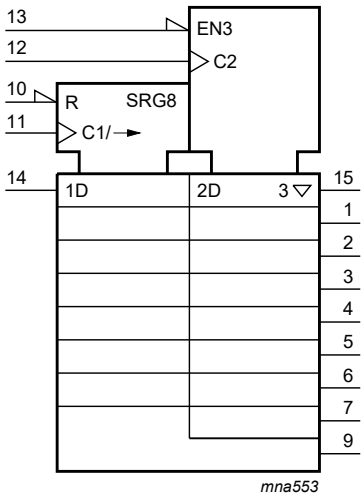


Fig. 3. IEC logic symbol

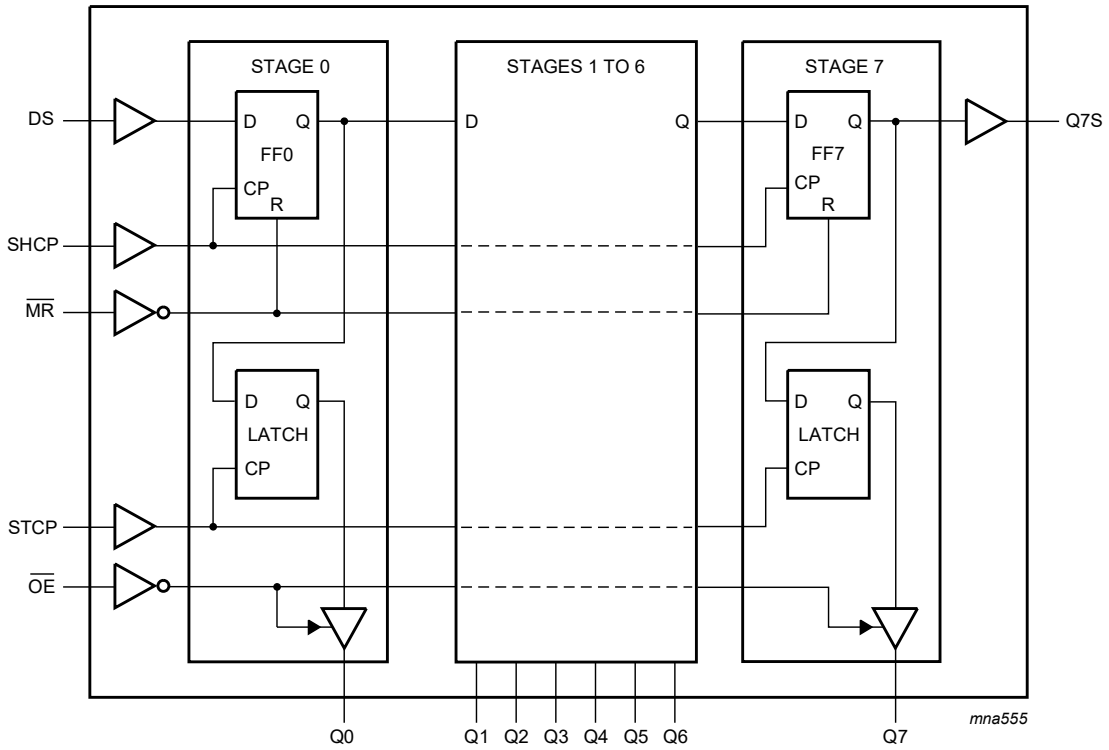


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning

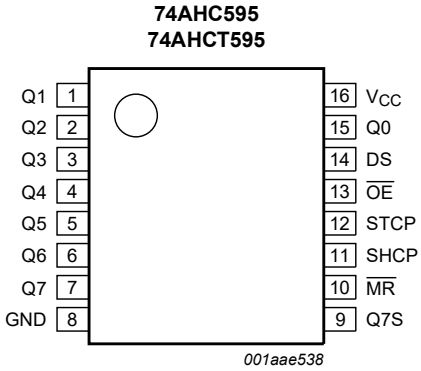
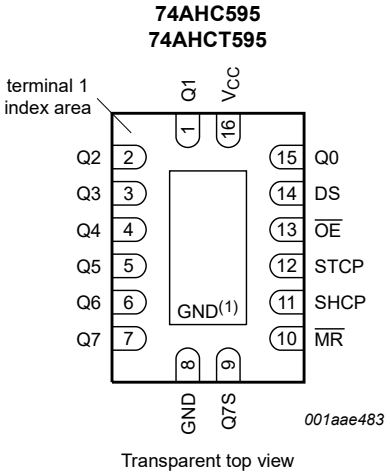


Fig. 5. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 6. Pin configuration SOT763-1 (DHVQFN16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{OE}$	13	output enable input (active LOW)
DS	14	serial data input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage state;
L = LOW voltage state;
↑ = LOW-to-HIGH transition;
X = don't care;
NC = no change;
Z = high-impedance OFF-state.

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

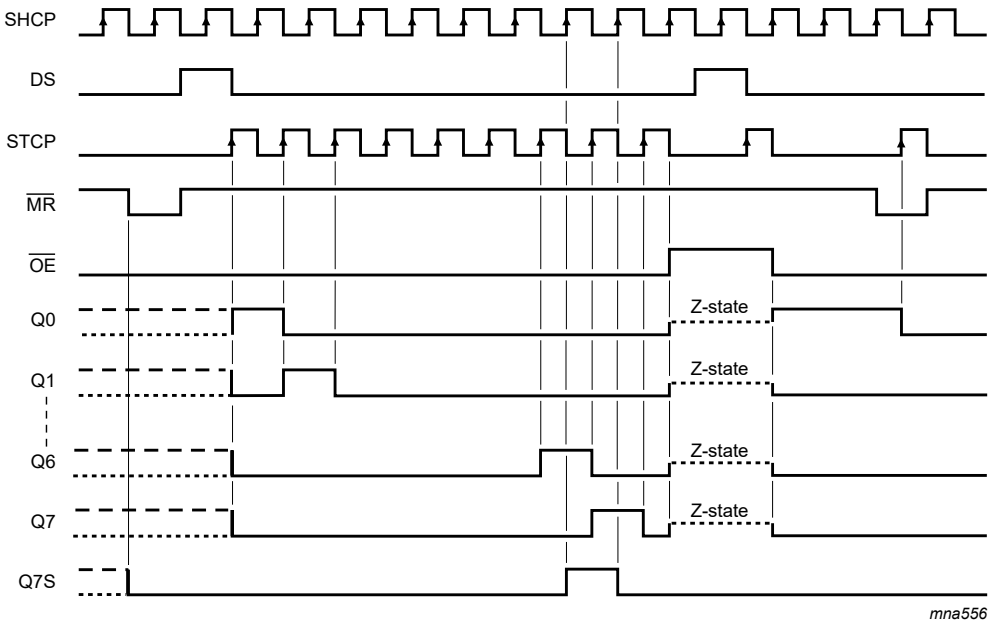


Fig. 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V	[1]	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	[1]	-20	+20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		-25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	74AHC595			74AHCT595			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	-	-	100	-	-	-	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC595										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
C_I	input capacitance		-	3	10	-	10	-	10	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT595										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3	10	-	10	-	10	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 13.

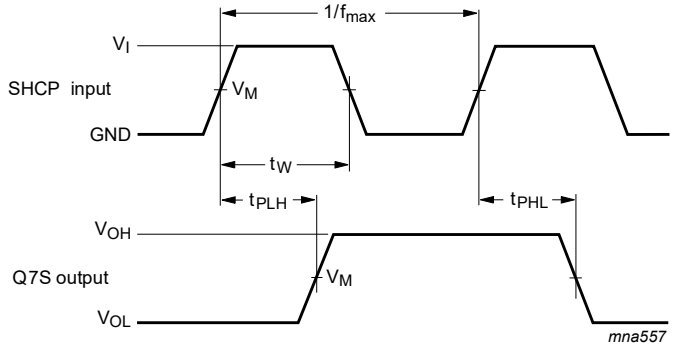
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHC595										
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 8 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.7	13.0	1.0	15.0	1.0	16.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.7	16.5	1.0	18.5	1.0	20.1	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.0	8.2	1.0	9.4	1.0	10.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.4	10.0	1.0	11.4	1.0	12.5	ns
		STCP to Qn; see Fig. 9 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.9	11.9	1.0	13.5	1.0	15.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.7	15.4	1.0	17.0	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.2	7.4	1.0	8.5	1.0	9.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.5	9.0	1.0	10.5	1.0	11.5	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 11								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.9	12.8	1.0	13.7	1.0	15.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.4	16.3	1.0	17.2	1.0	18.7	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.4	8.0	1.0	9.1	1.0	10.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.6	10.0	1.0	11.1	1.0	12.0	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 12 [3]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.6	11.5	1.0	13.5	1.0	15.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	7.4	15.0	1.0	17.0	1.0	18.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.0	8.6	1.0	10.0	1.0	11.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.3	10.6	1.0	12.0	1.0	13.0	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 12 [4]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	5.4	11.0	1.0	13.0	1.0	14.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	8.7	15.7	1.0	16.2	1.0	17.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	3.8	8.0	1.0	9.5	1.0	10.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f_{max}	maximum frequency	SHCP or STCP; see Fig. 8 and Fig. 9								
		V_{CC} = 3.0 V to 3.6 V	80	125	-	60	-	40	-	MHz
		V_{CC} = 4.5 V to 5.5 V	130	170	-	110	-	90	-	MHz
t_W	pulse width	SHCP HIGH or LOW; see Fig. 8								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Fig. 9								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{MR}$ LOW; see Fig. 11								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	DS to SHCP; see Fig. 10								
		V_{CC} = 3.0 V to 3.6 V	3.5	-	-	3.5	-	3.5	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Fig. 9								
		V_{CC} = 3.0 V to 3.6 V	8.5	-	-	8.5	-	8.5	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t_h	hold time	DS to SHCP; see Fig. 10								
		V_{CC} = 3.0 V to 3.6 V	1.5	-	-	1.5	-	1.5	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 11								
		V_{CC} = 3.0 V to 3.6 V	3.0	-	-	3.0	-	3.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.5	-	-	2.5	-	2.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [5] [6]	-	180	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHCT595										
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 8 [2]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	3.8	8.2	1.0	9.0	1.0	10.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.2	10.0	1.0	11.0	1.0	12.0	ns
		STCP to Qn; see Fig. 9 [2]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.0	7.4	1.0	8.5	1.0	9.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.3	9.0	1.0	10.5	1.0	11.5	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 11								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.6	8.2	1.0	9.5	1.0	10.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.8	10.5	1.0	11.5	1.0	12.5	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 12 [3]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.8	9.0	1.0	11.0	1.0	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	6.2	11.6	1.0	13.0	1.0	14.5	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 12 [4]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	3.6	6.9	1.0	8.0	1.0	9.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f_{max}	maximum frequency	SHCP and STCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 8 and Fig. 9	130	170	-	110	-	90	-	MHz
t_W	pulse width	SHCP HIGH or LOW; V_{CC} = 4.5 V to 5.5 V; see Fig. 8	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; V_{CC} = 4.5 V to 5.5 V; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{MR}$ LOW; V_{CC} = 4.5 V to 5.5 V; see Fig. 11	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	DS to SHCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 10	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
t_h	hold time	DS to SHCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 10	2.0	-	-	2.0	-	2.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; V_{CC} = 4.5 V to 5.5 V; see Fig. 11	3.0	-	-	3.0	-	3.0	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [5] [6]	-	190	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{en} is the same as t_{PZL} and t_{PZH}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.
[6] All 9 outputs switching.

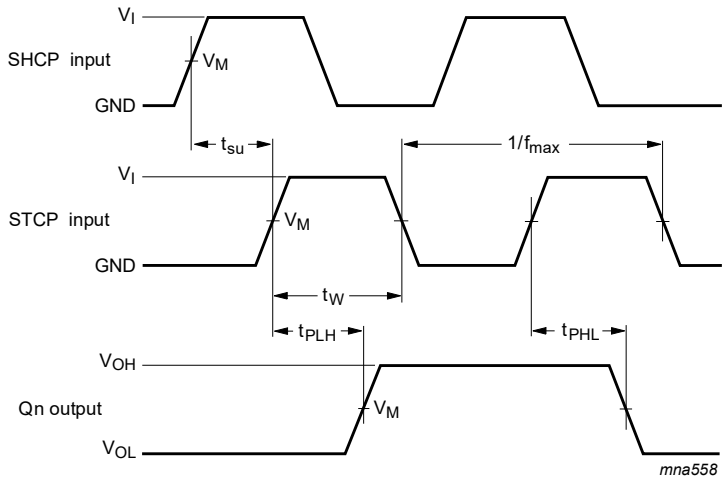
11.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

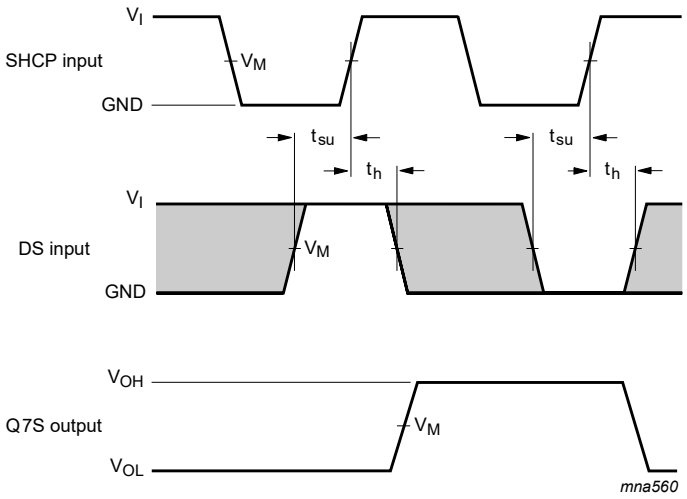
Fig. 8. Shift clock pulse, maximum frequency and input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Storage clock to output propagation delays

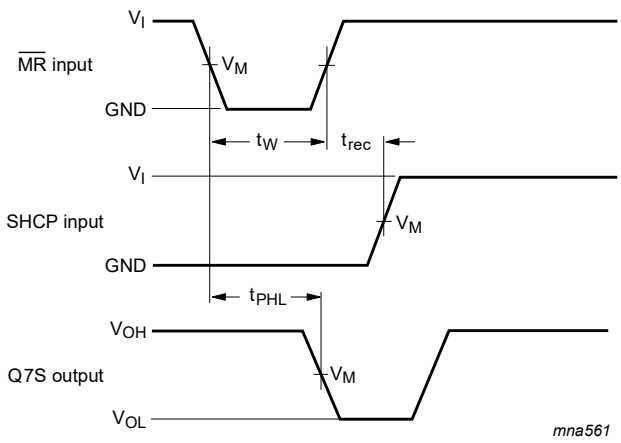


Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

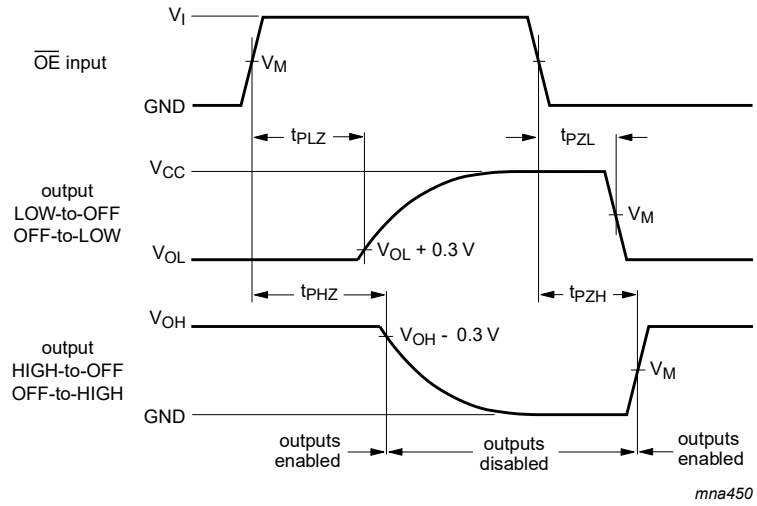
Fig. 10. Data set-up and hold times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 11. Master reset to output propagation delays



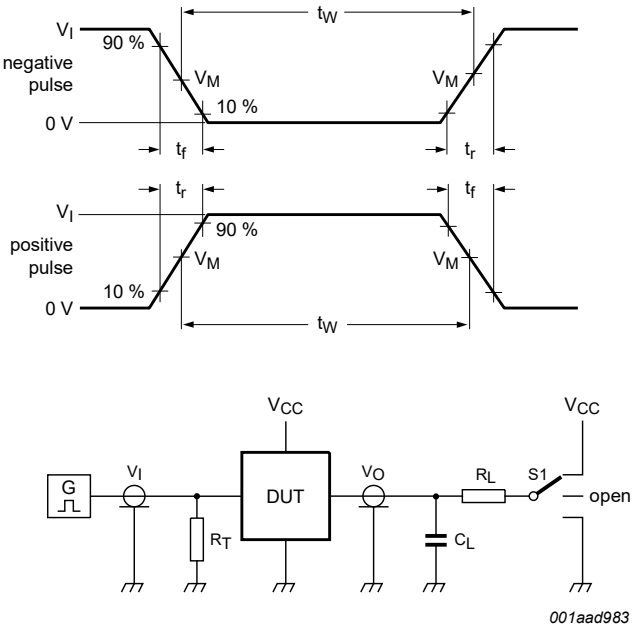
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 12. Enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC595	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT595	1.5 V	$0.5V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1 = test selection switch.

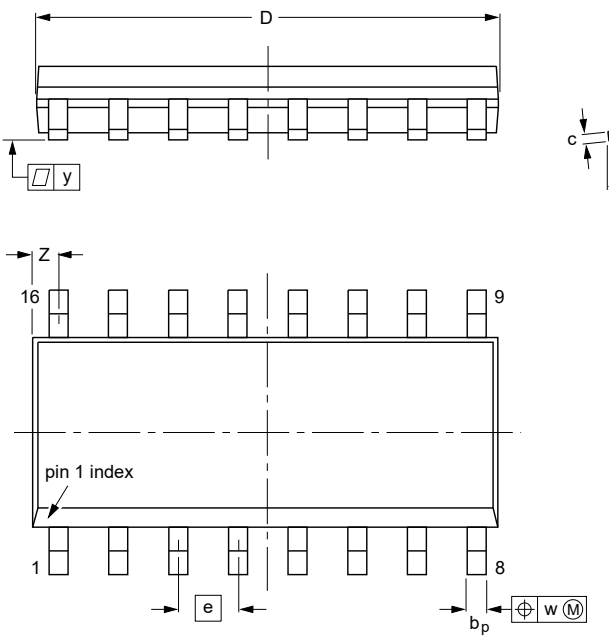
Fig. 13. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC595	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT595	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

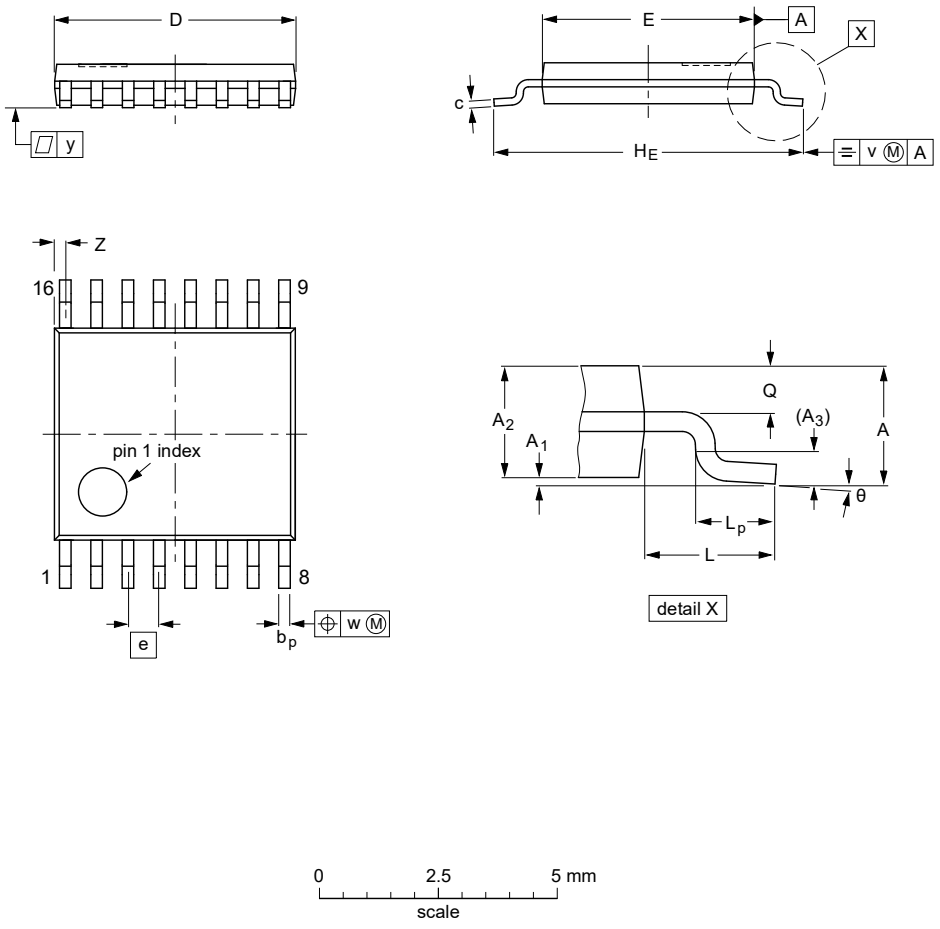
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

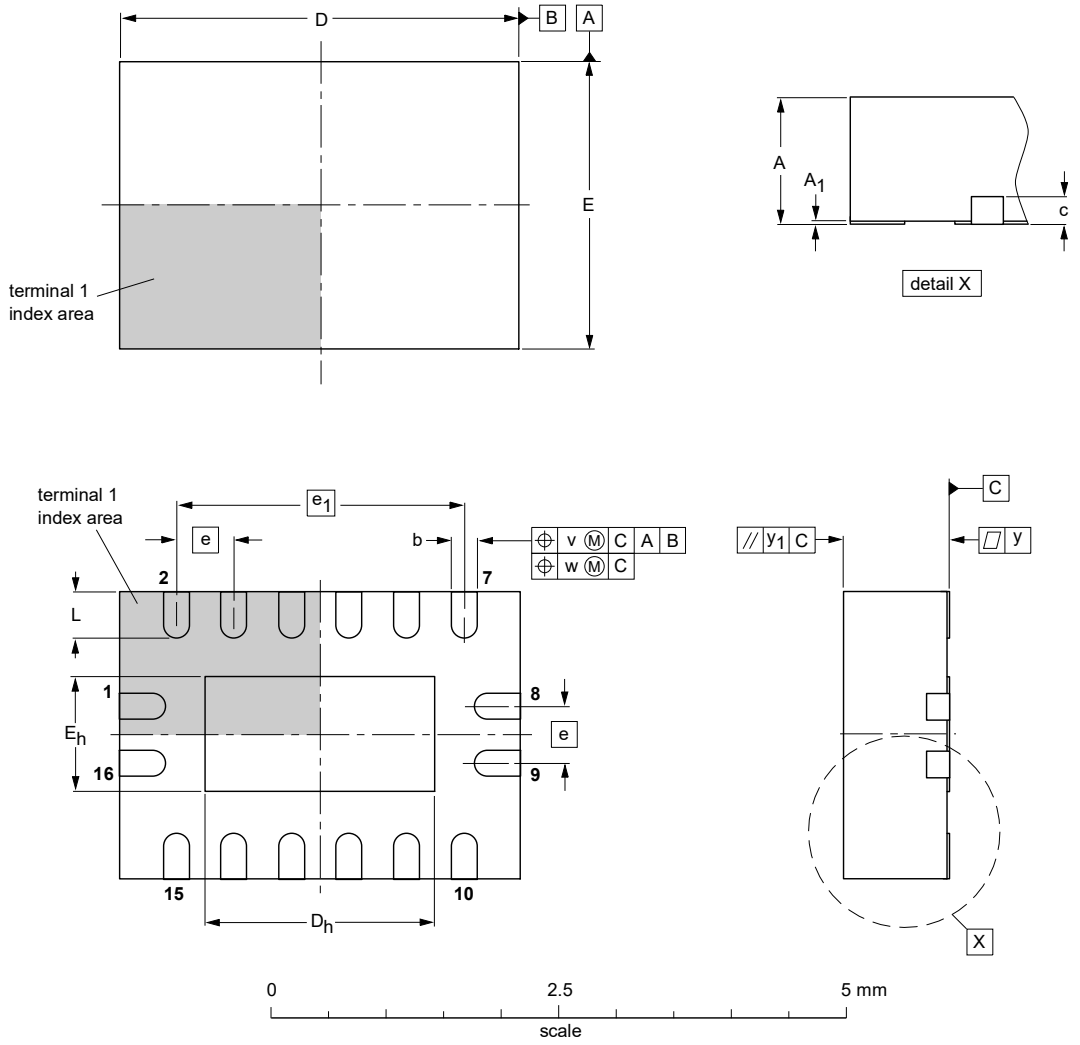
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 16. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT595 v.6	20200526	Product data sheet	-	74AHC_AHCT595 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Fig. 7: Timing diagram updated with SHCP waveform. • Table 4: Derating values for P_{tot} total power dissipation updated. • Table 7: Propagation delay symbol and parameter corrected (Errata).			
74AHC_AHCT595 v.5	20120704	Product data sheet	-	74AHC_AHCT595 v.4
Modifications:	• Added GND in the pin configuration drawing DHVQFN16 (errata)			
74AHC_AHCT595 v.4	20090811	Product data sheet	-	74AHC_AHCT595 v.3
74AHC_AHCT595 v.3	20080425	Product data sheet	-	74AHC_AHCT595 v.2
74AHC_AHCT595 v.2	20060323	Product data sheet	-	74AHC_AHCT595 v.1
74AHC_AHCT595 v.1	20000315	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 26 May 2020