DCPA10505, DCPA10505D
DCPA10512, DCPA10512D
DCPA10515, DCPA10515D

SBVS276A – APRIL 2017 – REVISED MAY 2020

DCPA1 Series, 1-W, 2000-V_{DC} Isolated, Unregulated DC/DC Converter Modules

1 Features

- 2-kVDC Isolation (operational): 1-second test
- Continuous voltage applied across isolation barrier: 60 VDC / 42.5 VAC
- UL1950 recognized component
- EN55022 class B EMC performance
- 7-Pin PDIP and 7-pin SOP packages
- Input voltage: 5 V ±10%
- Output voltage: ±5 V, ±12 V, or ±15 V
- Soft start to reduce in-rush current
- Frequency synchronization
- Thermal protection
- Short-circuit protected
- High efficiency

2 Applications

- Signal path isolation
- Ground loop elimination
- Data acquisition
- Industrial control and instrumentation
- Test equipment

3 Description

The DCPA1 series is a family of 1-W, isolated, unregulated DC/DC converter modules. Requiring a minimum of two external components, the DCPA1 series of devices include on-chip device protection, and the ability to synchronize to an external clock.

This combination of features and small size makes the DCPA1 series of devices suitable for a wide range of applications, and is an easy-to-use solution in applications requiring signal path isolation.

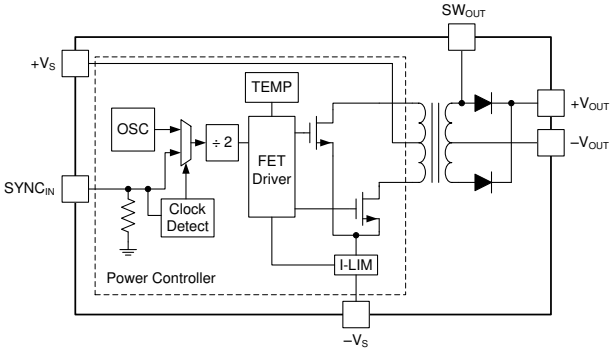
WARNING: This product has operational isolation and is intended for signal isolation only. It should not be used as a part of a safety isolation circuit requiring reinforced isolation. See definitions in *Feature Description*.

Device Information (1)

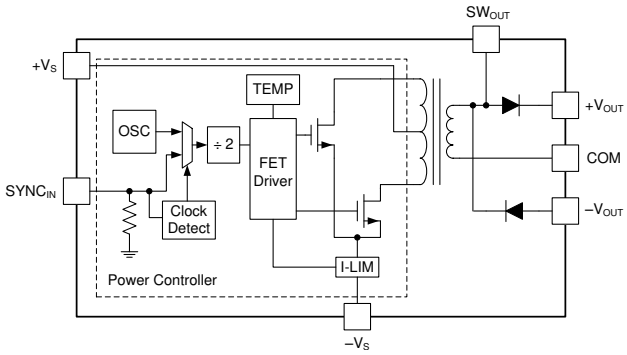
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DCPA1xxxx	PDIP (7)	19.18 mm × 10.60 mm
	SOP (7)	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Single Output Block Diagram



Dual Output Block Diagram



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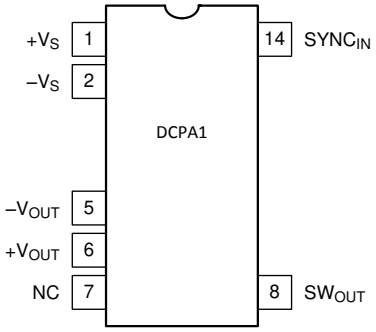
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

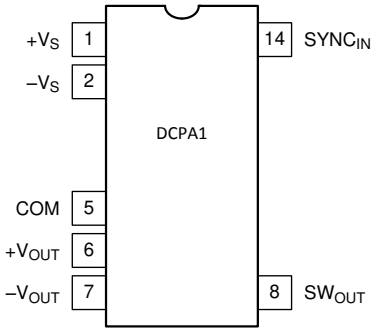
Changes from Original (April 2017) to Revision A	Page
• Added links to *Applications*	1

5 Pin Configuration and Functions

NVA and DUA Package
7-Pin PDIP and SOP (Single Output)
(Top View)



NVA and DUA Package
7-Pin PDIP and SOP (Dual Output)
(Top View)



Pin Functions

PIN NAME	PIN NUMBER		I/O (1)	Description
	SINGLE-OUTPUT	DUAL-OUTPUT		
COM	—	5	O	Output side common
NC	7	—	—	No connection
$SYNC_{IN}$	14	14	I	Synchronization. This pin is used to synchronize to an external clock. Internally it is pulled to GND. If valid clock is not detected on this pin, the SN6505 shifts automatically to internal clock.
SW_{OUT}	8	8	O	Unrectified transformer output
$+V_{OUT}$	6	6	O	Positive output voltage
$+V_S$	1	1	I	Input voltage
$–V_{OUT}$	5	7	O	Negative output voltage
$–V_S$	2	2	I	Input side common

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Input voltage	$+V_S$		–0.5	6	V
		50ns transient	–1.0	7	V
	$SYNC_{IN}$		–0.5	$+V_S$	V
		50ns transient	–1.0	6	V
Lead temperature (soldering, 10 s)				260	°C
Storage temperature, T_{stg}			–60	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage		4.5	5	5.5	V
Output power		0.05		1	W
Operating ambient temperature range		–40		100	°C

6.4 Electrical Characteristics

T_A = 25°C, $+V_S$ = nominal, C_{IN} = 2.2 µF, C_{OUT} = 1.0 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
P_{OUT}	Output power	Over $+V_S$ range, I_{OUT} = 100% (full load)				1	W
I_{OUT}	Output current		DCPA10505			200	mA
			DCPA10505D			200(1)	mA
			DCPA10512			83	mA
			DCPA10512D			83(1)	mA
			DCPA10515			66	mA
			DCPA10515D			66(1)	mA

(1) $I_{OUT1} + I_{OUT2}$

Electrical Characteristics (continued)

T_A = 25°C, $+V_S$ = nominal, C_{IN} = 2.2 µF, C_{OUT} = 1.0 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	I_{OUT} = 100% load (2)	DCPA10505		5.0		V
			DCPA10505D		±5.0		V
			DCPA10512		12.0		V
			DCPA10512D		±12.0		V
			DCPA10515		15.0		V
			DCPA10515D		±15.0		V
	Temperature variation	–40°C ≤ T_A ≤ 100°C, I_{OUT} = 100% load			0.02		%/°C
	Line regulation	$+V_S$(MIN) to $+V_S$(TYP), I_{OUT} = 10% load			10%		
		$+V_S$(TYP) to $+V_S$(MAX), I_{OUT} = 10% load			10%		
	Load regulation (3)	10% to 100% load			5%		
V_{RIPPLE}	Output voltage ripple (4)	C_{OUT} = 1 µF, I_{OUT} = 50%			20		mV_{PP}
INPUT							
$+V_S$	Input voltage range			4.5		5.5	V
UVLO	$+V_S$ Undervoltage lockout	$+V_S$ increasing threshold				2.25	V
		$+V_S$ decreasing threshold		1.7			V
I_Q	Quiescient current	I_{OUT} = 0% load	DCPA10505		35		mA
			DCPA10505D		25		mA
			DCPA10512		29		mA
			DCPA10512D		36		mA
			DCPA10515		31		mA
			DCPA10515D		38		mA

(2) See Load Regulation graphs in the Typical Characterization section for typical voltage at all load conditions.
(3) Load regulation = (V_{OUT} at 10% load – V_{OUT} at 100%)/V_{OUT} at 75% load
(4) Guaranteed by design. Not production tested.

Electrical Characteristics (continued)

T_A = 25°C, $+V_S$ = nominal, C_{IN} = 2.2 µF, C_{OUT} = 1.0 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISOLATION							
V_{ISO}	Isolation	1-second flash test, voltage	DC	2.0 (5) (4)			kVDC
			AC	1.5 (5)			kVrms
		1-second flash test, leakage current				30	µA
		Continuous working voltage across isolation barrier	DC			60	VDC
			AC			42.5	VAC
			dV/dt			50	V/ms
C_{ISO}	Barrier capacitance	V_{ISO} = 750 Vrms			28		pF
PERFORMANCE							
	Efficiency	I_{OUT} = 100%	DCPA10505		85%		
			DCPA10505D		85%		
			DCPA10512		87%		
			DCPA10512D		88%		
			DCPA10515		86%		
			DCPA10515D		86%		
	Transient response (4)	50% to 100% load step	DCPA10505		3.0%		
			DCPA10512		1.9%		
			DCPA10515		2.0%		
		50% to 100% load step per output (6)	DCPA10505D		2.7%		
			DCPA10512D		2.0%		
			DCPA10515D		1.6%		
RELIABILITY							
	Demonstrated	T_A = 55°C			55		FITS
CAPACITANCE							
C_{IN}	External input capacitance	Ceramic		2.2			µF
C_{OUT}	External output capacitance	Ceramic		0.1	1.0	200	µF
THERMAL SHUTDOWN							
T_{SD}	Die temperature at shutdown				168		°C
I_{SD}	Shutdown current				3		mA

(5) See Isolation Voltage section for more information.
(6) Transient testing for dual output devices are tested with one output loaded with a 50% static load and the other output loaded with a 50% to 100% dynamic load step.

6.5 Switching Characteristics

at T_A = +25°C, $+V_S$ = nominal, C_{IN} = 2.2 µF, C_{OUT} = 1.0 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	$f_{SW} = f_{OSC}/2$		850		kHz
f_{SYNC}	Synchronization frequency range		750		1000	kHz
V_{IH}	High-level input threshold, $SYNC_{IN}$		0.7			V
V_{IL}	Low-level input threshold, $SYNC_{IN}$				0.3	V

6.6 Typical Characteristics (DCPA10505)

At T_A = 25°C, $+V_S$ = nominal, (unless otherwise noted)

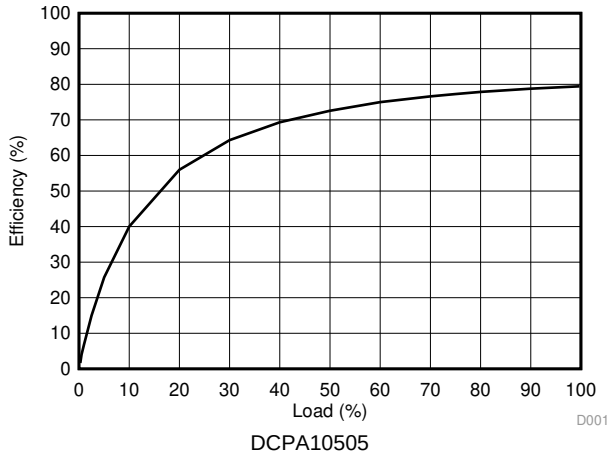


Figure 1. Efficiency versus Load

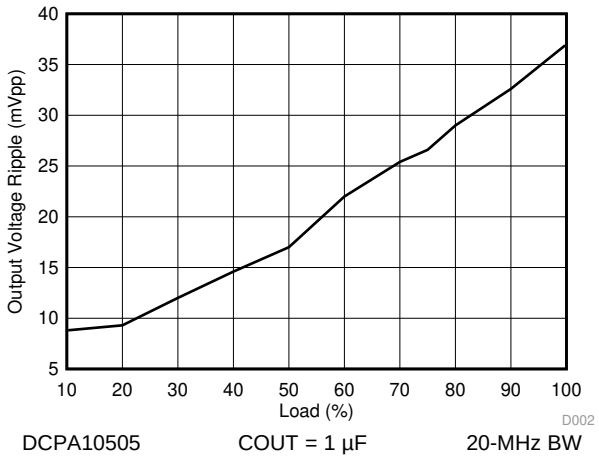


Figure 2. Output Ripple versus Load

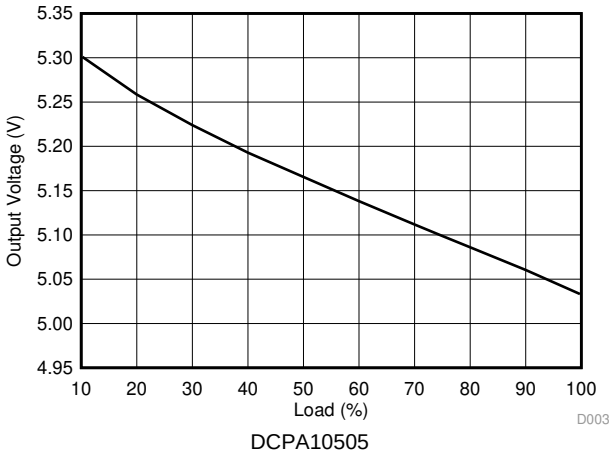


Figure 3. Load Regulation

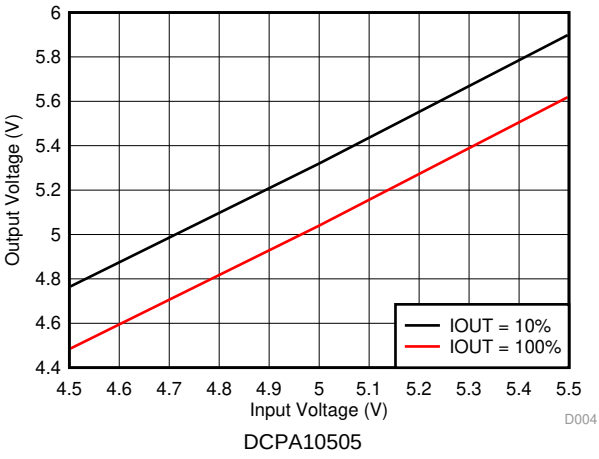


Figure 4. Line Regulation

6.7 Typical Characteristics (DCPA10512)

At T_A = 25°C, $+V_S$ = nominal, (unless otherwise noted)

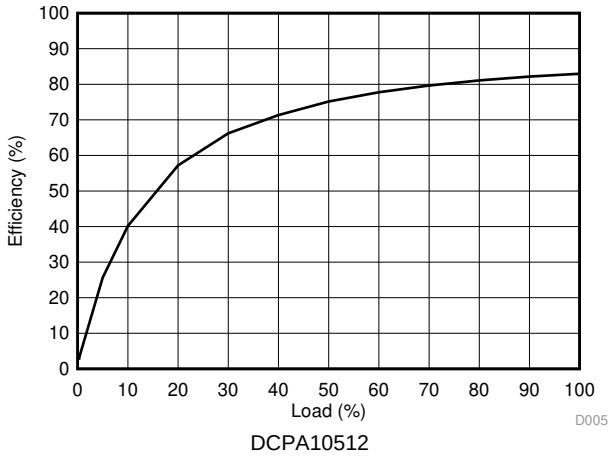


Figure 5. Efficiency versus Load

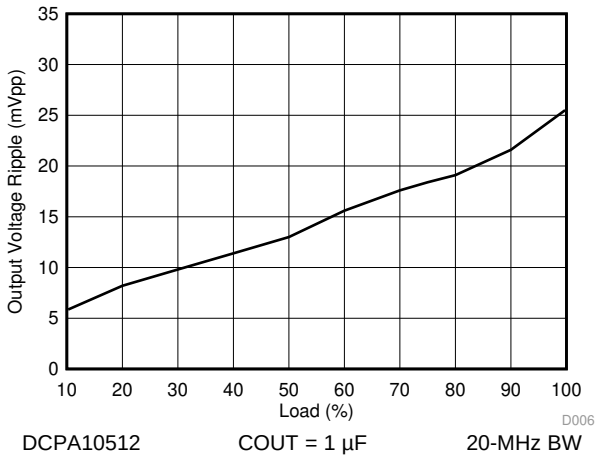


Figure 6. Output Ripple versus Load

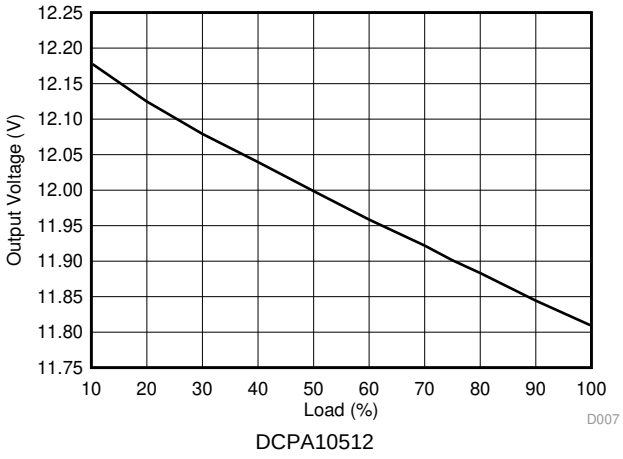


Figure 7. Load Regulation

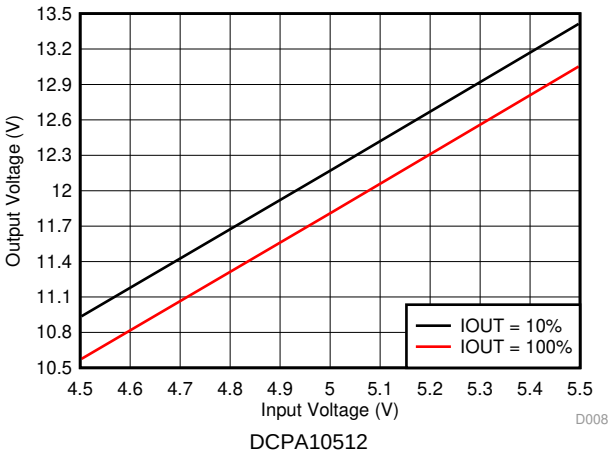


Figure 8. Line Regulation

6.8 Typical Characteristics (DCPA10515)

At T_A = 25°C, $+V_S$ = nominal, (unless otherwise noted)

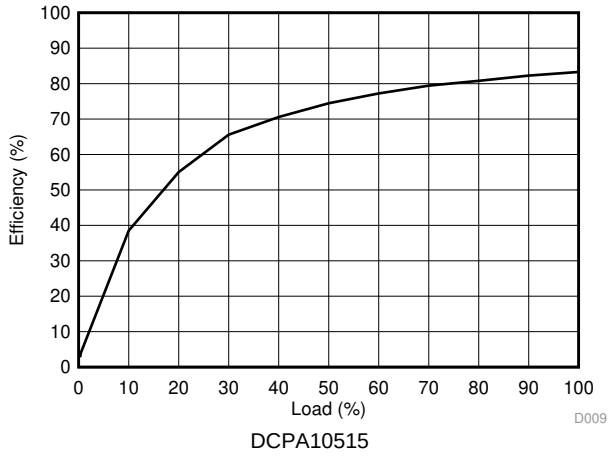


Figure 9. Efficiency versus Load

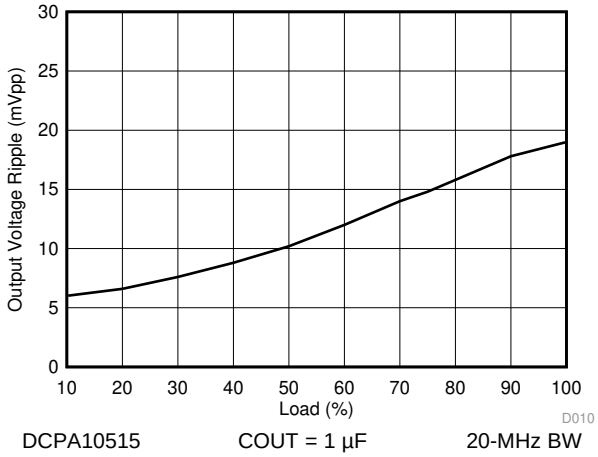


Figure 10. Output Ripple versus Load

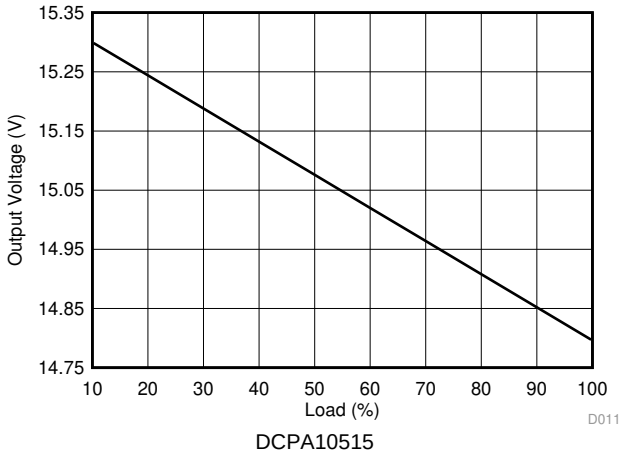


Figure 11. Load Regulation

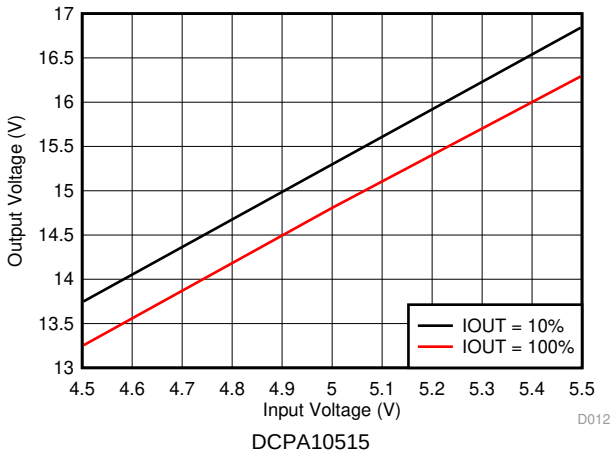


Figure 12. Line Regulation

6.9 Typical Characteristics (DCPA10505D)

At T_A = 25°C, $+V_S$ = nominal, (unless otherwise noted)

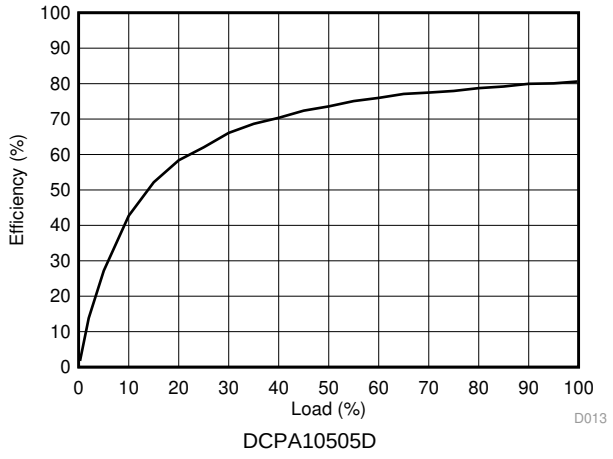


Figure 13. Efficiency versus Load

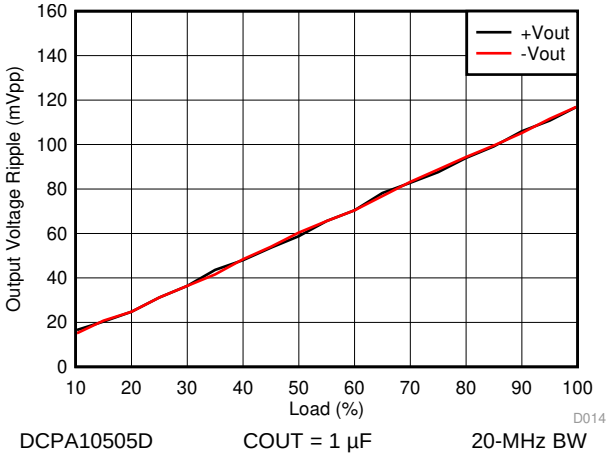


Figure 14. Output Ripple versus Load

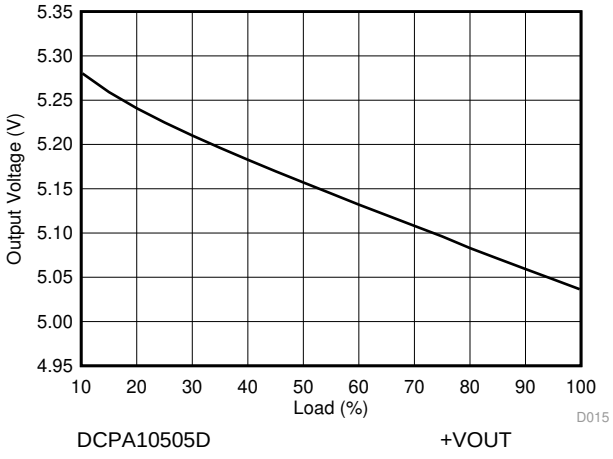


Figure 15. +VOUT Load Regulation

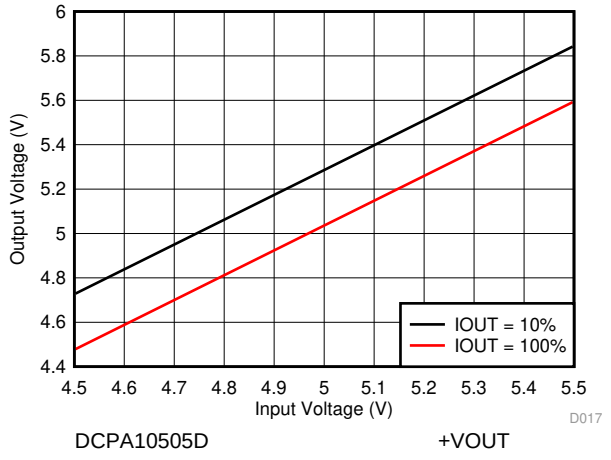


Figure 16. +VOUT Line Regulation

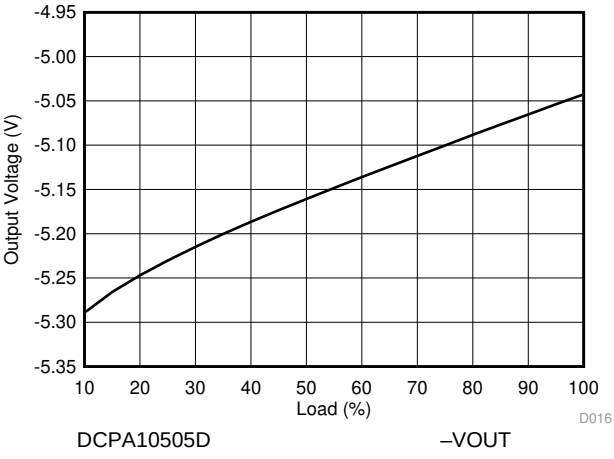


Figure 17. –VOUT Load Regulation

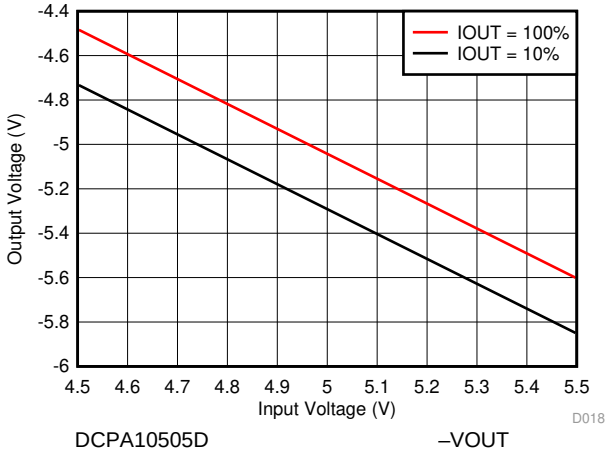


Figure 18. –VOUT Line Regulation

6.10 Typical Characteristics (DCPA10512D)

At T_A = 25°C, $+V_S$ = nominal, (unless otherwise noted)

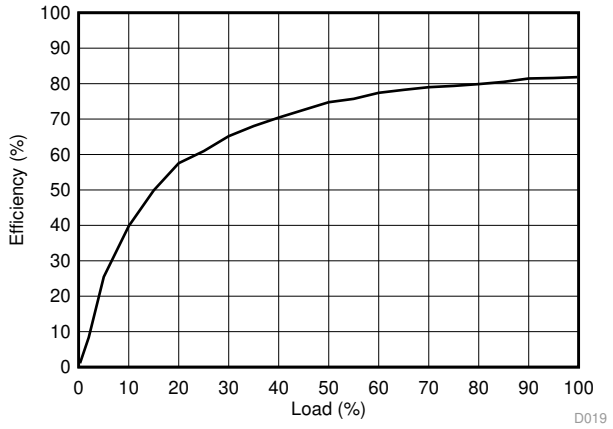


Figure 19. Efficiency versus Load

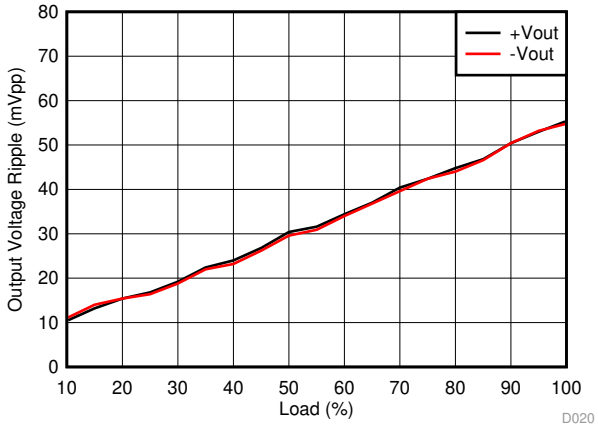


Figure 20. Output Ripple versus Load

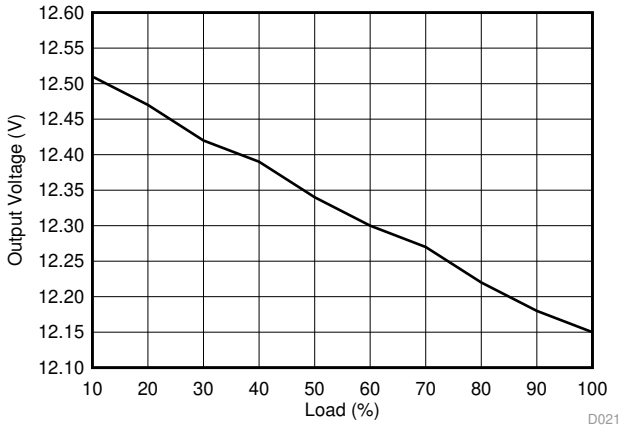


Figure 21. +VOUT Load Regulation

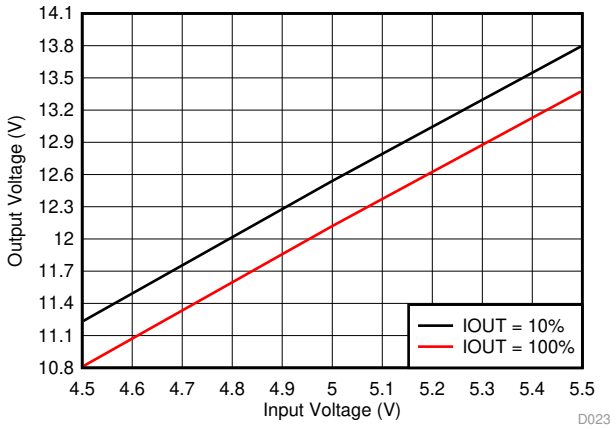


Figure 22. +VOUT Line Regulation

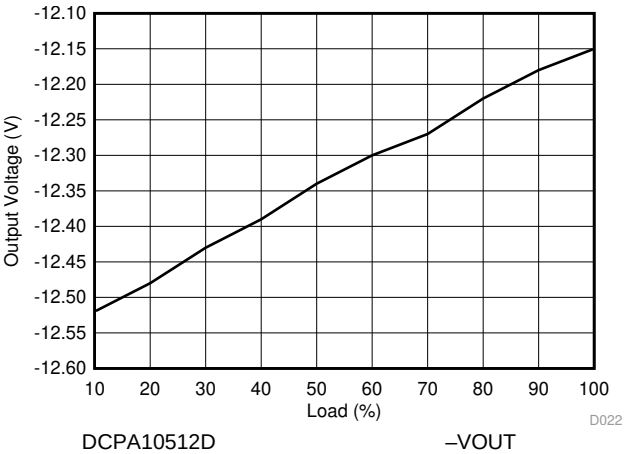


Figure 23. –VOUT Load Regulation

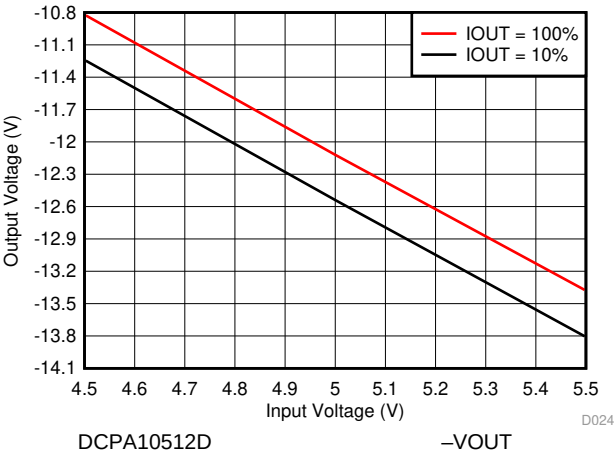


Figure 24. –VOUT Line Regulation

6.11 Typical Characteristics (DCPA10515D)

At T_A = 25°C, $+V_S$ = nominal, (unless otherwise noted)

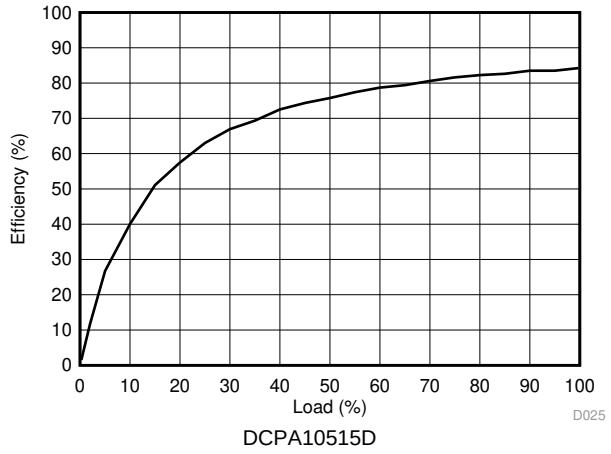


Figure 25. Efficiency versus Load

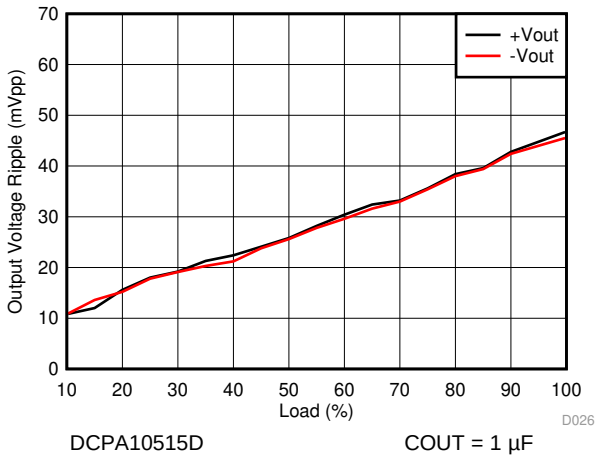


Figure 26. Output Ripple versus Load

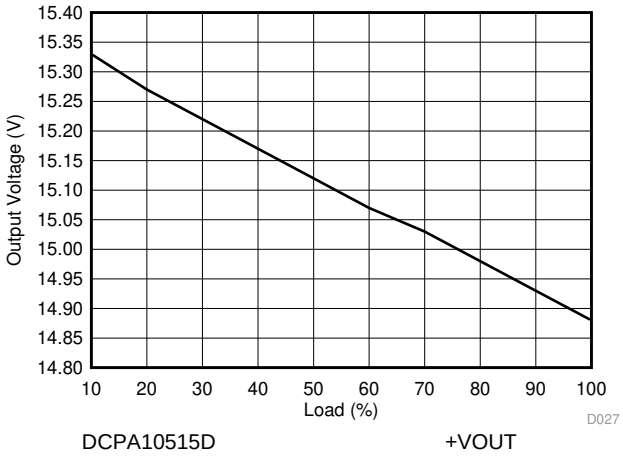


Figure 27. +VOUT Load Regulation

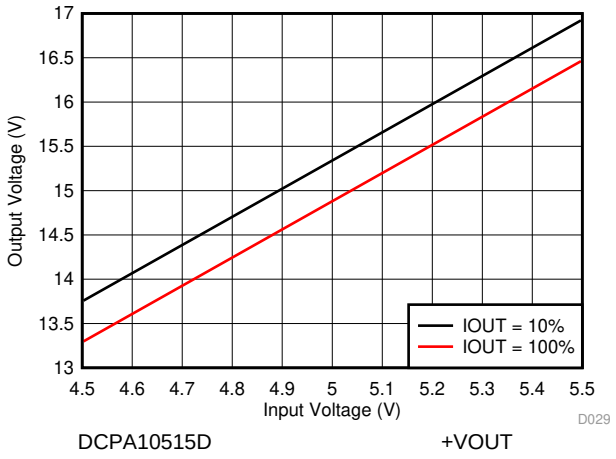


Figure 28. +VOUT Line Regulation

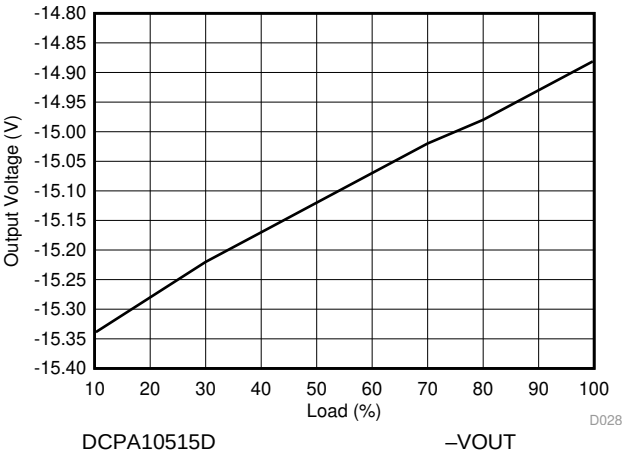


Figure 29. –VOUT Load Regulation

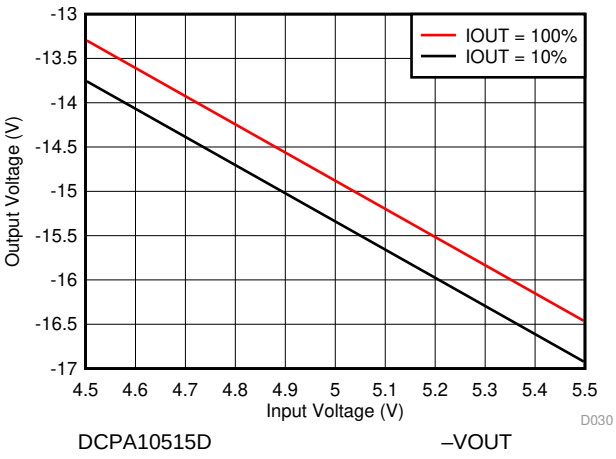


Figure 30. –VOUT Line Regulation

7 Detailed Description

7.1 Overview

The DCPA1 offers up to 1 W of isolated, unregulated output power from a 5-V input source with a typical efficiency of up to 87%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control device. The DCPA1 devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS and DMOS process.

7.2 Functional Block Diagrams

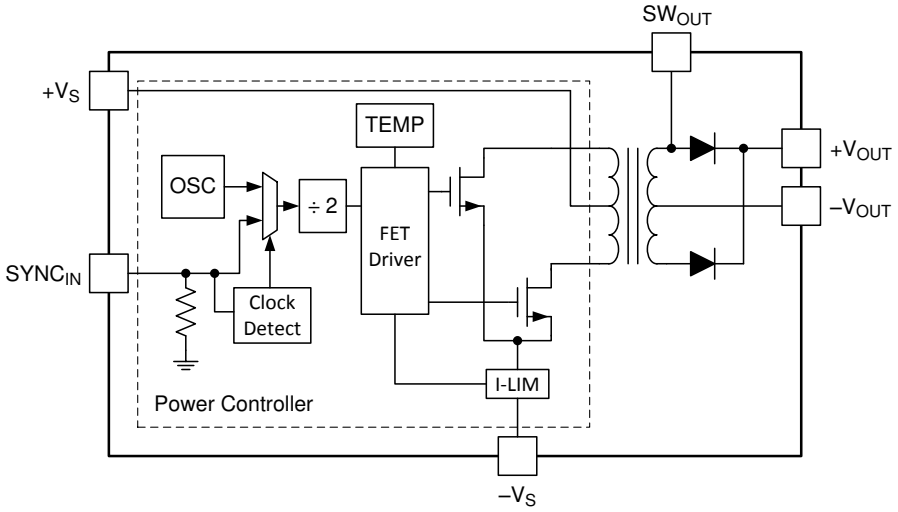


Figure 31. Single Output Device

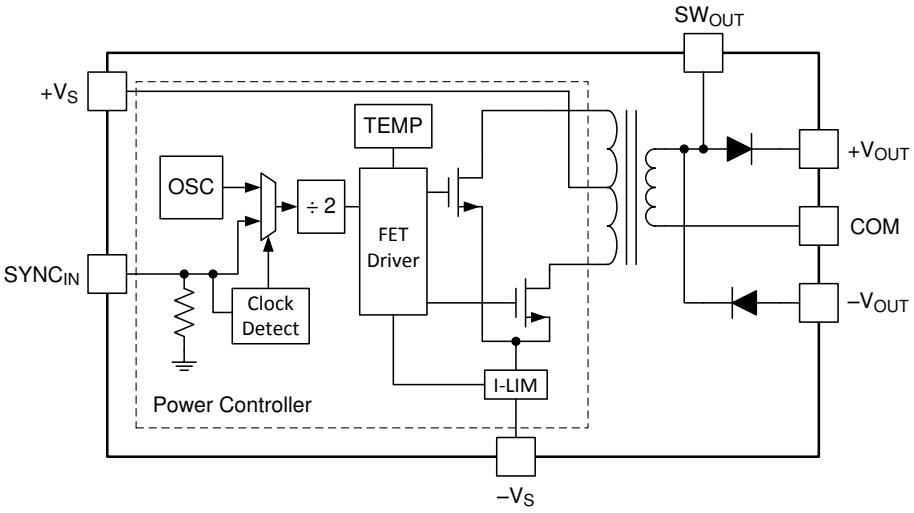


Figure 32. Dual Output Device

7.3 Feature Description

7.3.1 Isolation

Underwriters Laboratories, UL™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42 V peak or 60 V_{DC} for more than 1 second.

7.3.1.1 Operation or Functional Isolation

Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation should never be used as an element in a safety-isolation system.

7.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

7.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.4 V_{RMS}, or 60 V_{DC}. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

WARNING

Do not use the device as an element of a safety isolation system that exceeds the SELV limit.

If the device is expected to function correctly with more than 42.4 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

7.3.1.4 Isolation Voltage

The terms *Hipot test*, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* all describe the same spec. The terms describe a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCPA1 series of dc-dc converters are all 100% production tested at 1.5 kV_{AC} for one second.

7.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCPA1 series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

Feature Description (continued)

7.3.2 Power Stage

The DCPA1 series of devices uses a push-pull, center-tapped topology. The DCPA1 devices switch at 425 kHz (divide-by-2 from an 850-kHz oscillator).

7.3.3 Input and Output Capacitors

For all DCPA1 designs, a minimum 2.2-µF, low-ESR, ceramic input capacitor is required. Place the input capacitor as close as possible to the device input pins, $+V_S$ and $-V_S$, to ensure good start-up performance.

The recommended typical output capacitance for each output of any DCPA1 device is 1.0-µF of low-ESR, ceramic capacitance. Adding additional output capacitance will aid in ripple reduction, however, any additional capacitance will also require additional input current at start-up.

7.3.4 Oscillator And Watchdog Circuit

The onboard, 850-kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to an external source, and is used to minimize system noise. A watchdog circuit checks the operation of the oscillator circuit.

7.3.5 Synchronization

When more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCPA1 series of devices overcomes this interference by allowing devices to synchronize to an external clock. The $SYNC_{IN}$ pin responds to the rising edge of the external clock. If the external clock is removed, the DCPA1 will return to the frequency of the internal oscillator. If unused, it is recommended to connect this pin to the input side common, $-V_S$.

7.3.6 SW_{OUT}

The SW_{OUT} pin is directly connected to one winding of the transformer secondary prior to the output rectifier. It is not recommended to pull current from this pin. Do not connect capacitance directly to this pin as it will degrade performance. The SW_{OUT} pin is not compatible with the $SYNC_{IN}$ pin, therefore these two pins should not be connected together.

7.3.7 Soft Start

The DCPA1 series of devices includes a soft-start feature that prevents high in-rush current during power up. Once input power is applied, there is a delay of typically 10 ms before the output voltage begins to rise. Once the output voltage begins to rise, the soft-start time is typically 5 ms.

7.3.8 Load Regulation

The load regulation of the DCPA1 series of devices is specified at 10% to 100% load. Operation below 10% load can cause the output voltage to increase up to 40% higher than the typical output voltage. Placing a minimum 10% load ensures the output voltage is within the range specified in the *Electrical Characteristics*.

Feature Description (continued)

7.3.9 Thermal Performance

The DCPA1 family of devices have been characterized to operate over an ambient temperature range of –40°C to +100°C. The Safe Operating Area curve shown in Figure 33 represents the operating conditions of the DCPA1 devices where the maximum thermal ratings will not be exceeded. Figure 33 shows that all DCPA1 devices can safely operate over the full ambient temperature range, without airflow, to the full current rating of the device.

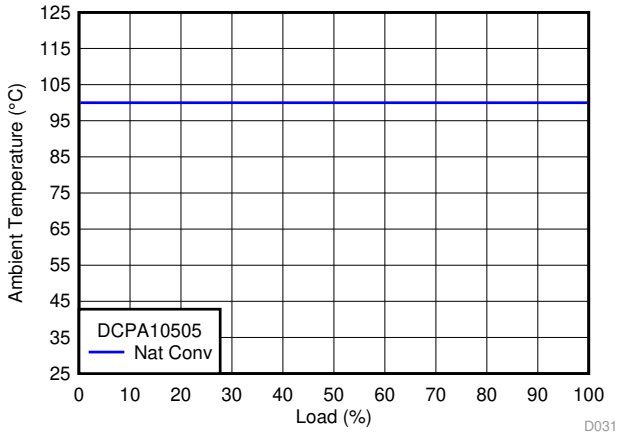


Figure 33. Thermal Safe Operating Area

7.3.9.1 Thermal Protection

The DCPA1 series of devices are protected by a thermal-shutdown circuit.

If the on-chip temperature rises above 150°C, the device shuts down. Normal operation resumes as soon as the temperature falls below 150°C. While the overtemperature condition continues, operation randomly cycles on and off. This cycling continues until the temperature is reduced.

7.3.10 Current Limit

For protection against a short circuit on the output, the DCPA1 series of devices have a built in current limit protection threshold of 1.75A (typical). These devices are not intended to be used at output currents greater than the output current rating of the device as shown in the *Electrical Characteristics*. Operating at currents greater than the device's current rating, but less than current limit threshold will cause excessive stress to the internal components. For protection against a partial short circuit condition, an input fuse or output fuse is recommended.

7.3.11 Construction

The basic construction of the DCPA1 series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCPA1 series of devices are constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Because the package contains no solder, the devices do not require any special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Ripple Reduction

The high switching frequency of 425 kHz allows simple filtering. To reduce output voltage ripple, it is recommended that a minimum of 1-µF capacitor be used on the $+V_{OUT}$ pin. For dual output devices, decouple both of the outputs to the COM pin. The required 2.2-µF, low ESR ceramic input capacitor also helps to reduce ripple and noise. See the *DC-to-DC Converter Noise Reduction Application Report*.

8.1.2 Connecting the DCPA1 in Series

Multiple DCPA1 isolated 1-W DC/DC converters can be connected in series to provide non-standard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCPA1 devices by connecting the $+V_{OUT}$ from one DCPA1 to the $-V_{OUT}$ of another as shown in Figure 34. The synchronization feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

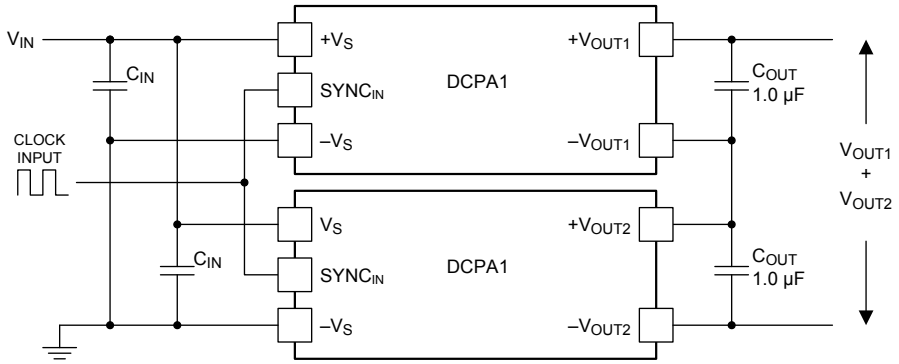


Figure 34. Multiple DCPA1 Devices Connected in Series

The outputs of a dual-output DCPA1 device can also be connected in series to provide two times the magnitude of $+V_{OUT}$, as shown in Figure 35. For example, connect a dual-output, ±15-V, DCPA10515D device to provide a 30-V rail.

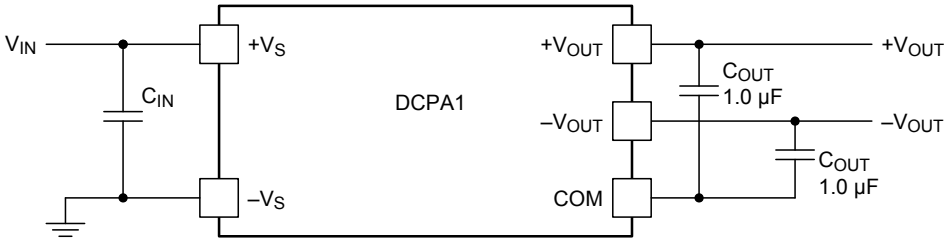


Figure 35. Dual Output Devices Connected in Series

8.1.3 Connecting the DCPA1 in Parallel

If the output power from one DCPA1 is not sufficient, it is possible to parallel the outputs of multiple DCPA1s, as shown in Figure 36 (applies to single output devices only). The synchronization feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

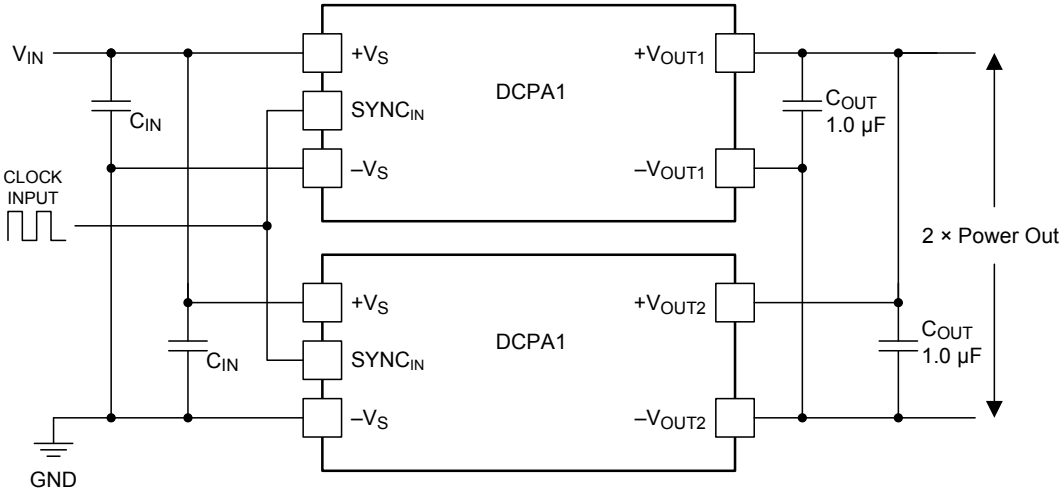


Figure 36. Multiple DCPA1 Devices Connected in Parallel

8.2 Typical Application

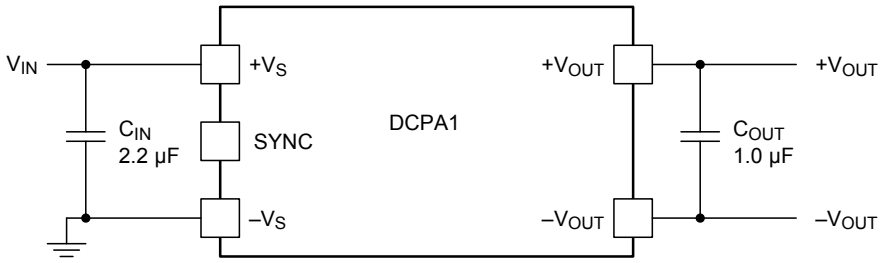


Figure 37. Typical DCPA10505 Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 and follow the design procedures shown in the *Detailed Design Procedure*.

Table 1. Design Example Parameters

PARAMETER		VALUE	UNIT
$V_{(+VS)}$	Input voltage	5	V
$V_{(+VOUT)}$	Output voltage	5	V
I_{OUT}	Output current rating	200	mA
f_{SW}	Operating frequency	425	kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

For all DCPA1, 5-V input voltage designs, select a 2.2-µF low-ESR ceramic input capacitor to ensure a good startup performance.

8.2.2.2 Output Capacitor

For any DCPA1 design, select a 1.0-µF low-ESR ceramic output capacitor to reduce output ripple.

8.2.2.3 $SYNC_{IN}$ Pin

In a stand-alone application, it is recommended to connect this pin to the input side common, $–V_S$.

8.2.3 PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes where possible. If that is not possible, use wide traces to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the traces must be deployed. Do not connect the devices in series, because that type of connection cascades the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See the *PCB Layout* section for more details.

8.2.4 DCPA10505 Application Curves

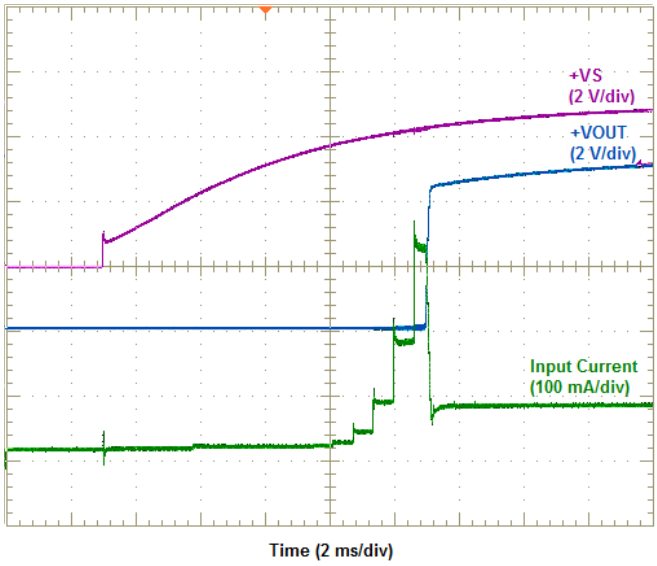


Figure 38. DCPA10505 Turn-ON

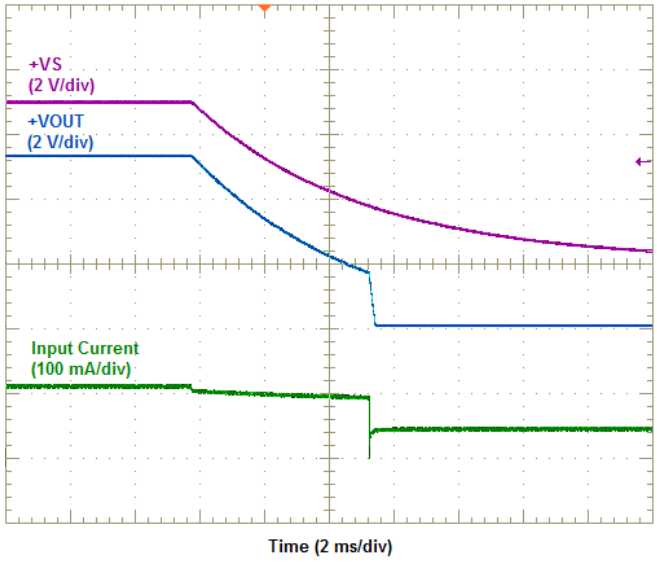


Figure 39. DCPA10505 Turn-OFF

9 Power Supply Recommendations

The DCPA1 is a switching power supply, and as such, can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to connect the power to the input of DCPA1 device. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

10 Layout

10.1 Layout Guidelines

Due to the high power density of these devices, provide ground planes on the input and output rails.

Figure 40 shows the schematic for a single output DCPA1 device. Figure 40 illustrates a printed circuit board (PCB) layout for the schematics.

Including input power and ground planes provides a low-impedance path for the input power. For the output, the COM signal connects via a ground plane, while the connections for the positive and negative voltage outputs conduct via wide traces to minimize losses.

The output should be taken from the device using ground and power planes, thereby ensuring minimum losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

If the $SYNC_{IN}$ pin is unused, it is recommended to connect this pin to the input side common, $–V_S$. Allow the SW_{OUT} pin to remain configured as a floating pad.

10.2 Layout Example

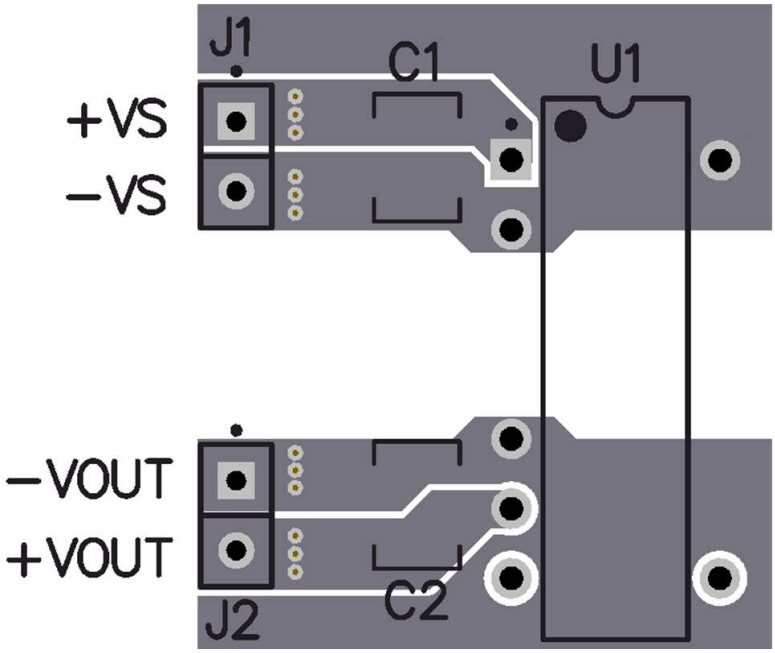


Figure 40. Typical Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

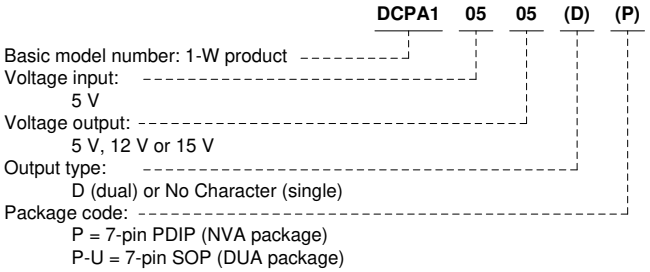


Figure 41. Supplemental Ordering Information

11.2 Documentation Support

11.2.1 Related Documentation

DC-to-DC Converter Noise Reduction

External Synchronization of the DCP01/02 Series of DC/DC Converters

Optimizing Performance of the DCP01/02 Series of DC/DC Converters

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DCPA10505	Click here	Click here	Click here	Click here	Click here
DCPA10505D	Click here	Click here	Click here	Click here	Click here
DCPA10512	Click here	Click here	Click here	Click here	Click here
DCPA10512D	Click here	Click here	Click here	Click here	Click here
DCPA10515	Click here	Click here	Click here	Click here	Click here
DCPA10515D	Click here	Click here	Click here	Click here	Click here

11.5 Trademarks

E2E is a trademark of Texas Instruments.
Underwriters Laboratories, UL are trademarks of UL LLC.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCPA10505DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10505DP	Samples
DCPA10505DP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10505DP-U	Samples
DCPA10505P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10505P	Samples
DCPA10505P-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10505P-U	Samples
DCPA10512DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10512DP	Samples
DCPA10512DP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10512DP-U	Samples
DCPA10512P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10512P	Samples
DCPA10512P-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10512P-U	Samples
DCPA10515DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10515DP	Samples
DCPA10515DP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10515DP-U	Samples
DCPA10515P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCPA10515P	Samples
DCPA10515P-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCPA10515P-U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

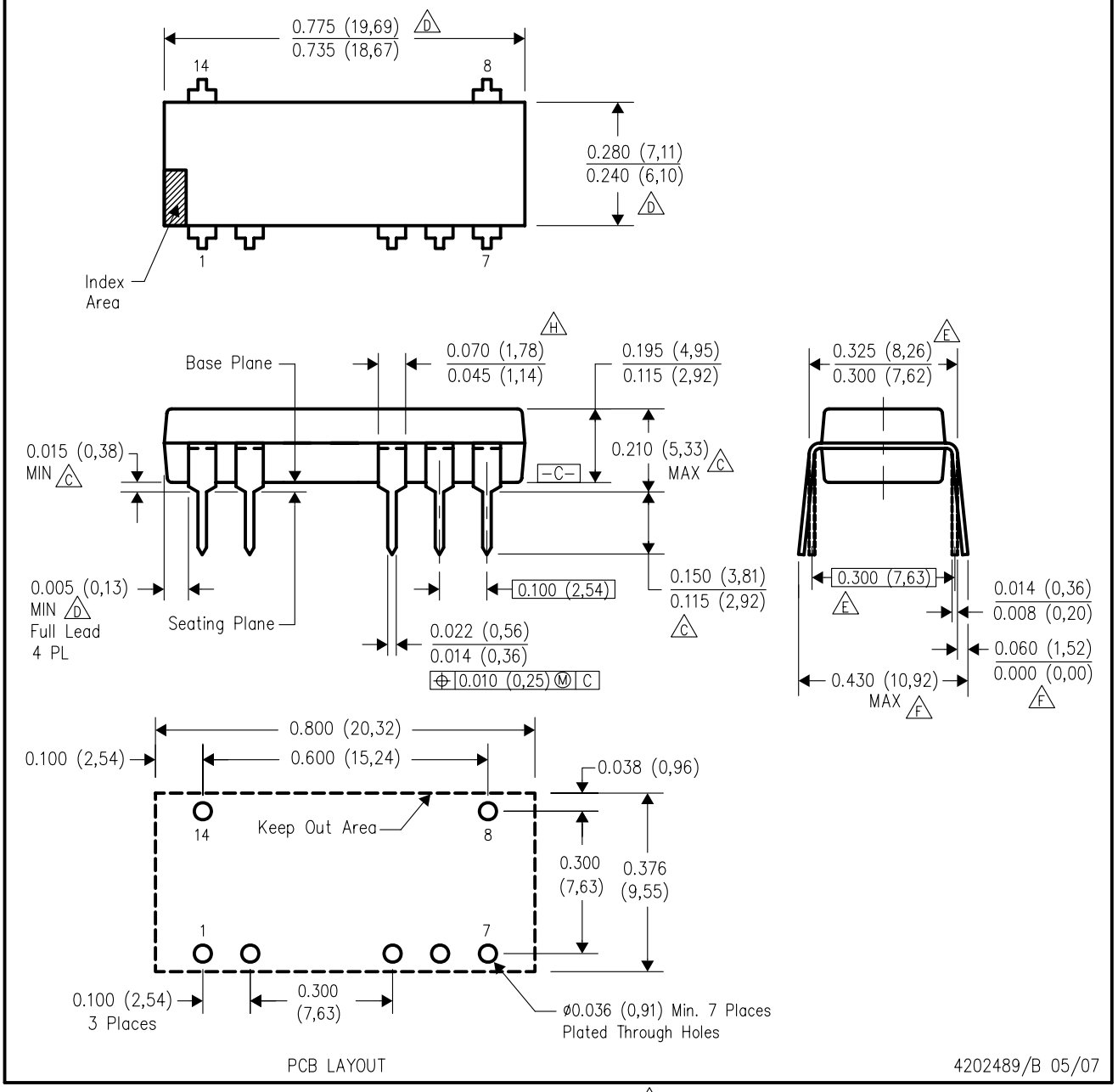
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

NVA (R–PDIP–T7/14) PLASTIC DUAL–IN–LINE

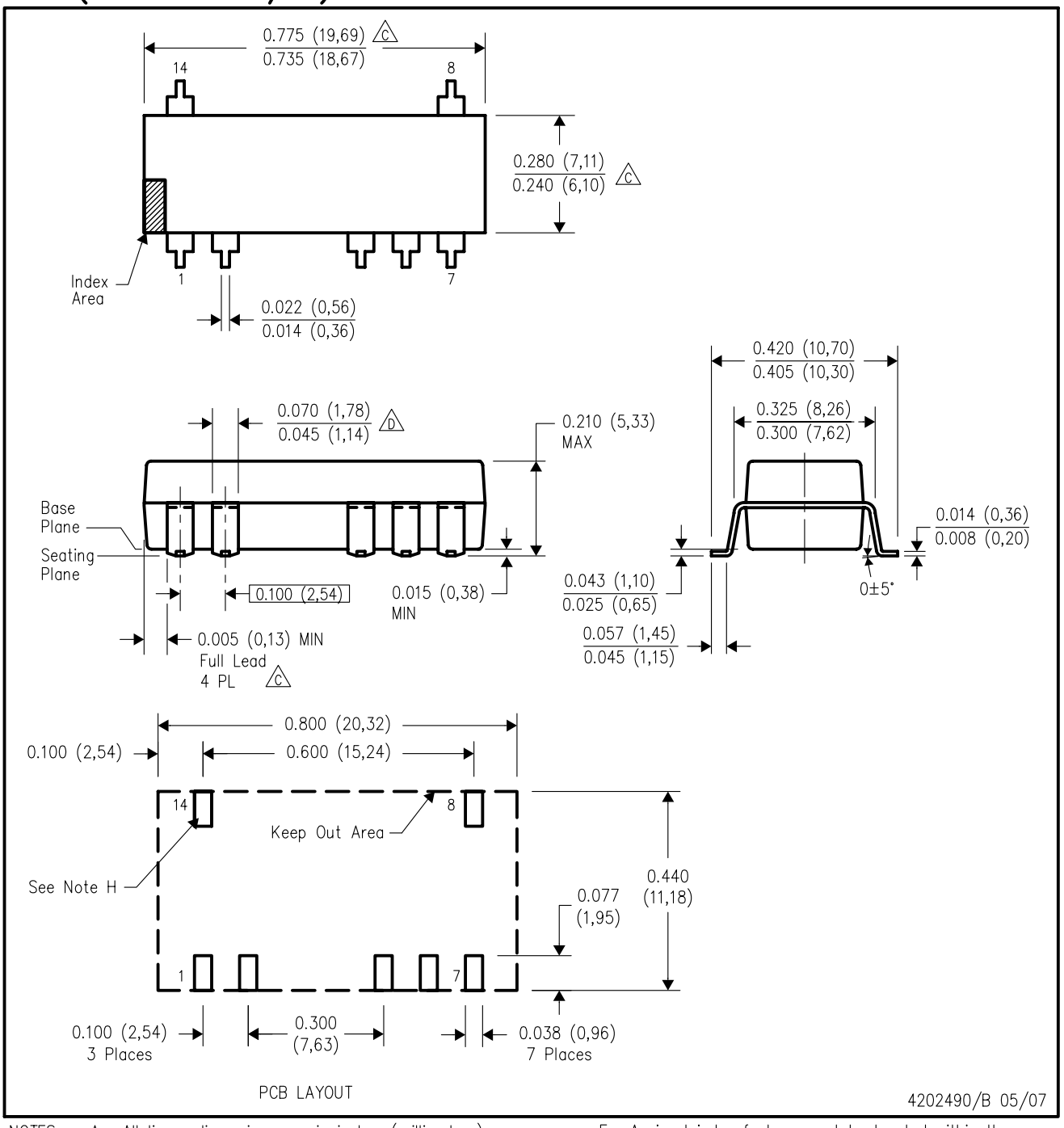


PCB LAYOUT

4202489/B 05/07

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS–3.
- D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
- F. Dimensions are measured at the lead tips with the leads unconstrained.
- G. Pointed or rounded lead tips are preferred to ease insertion.
- H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
- I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- J. A visual index feature must be located within the cross–hatched area.
- K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- L. Falls within JEDEC MS–001–AA.

DUA (R–PDSO–G7/14) PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- D. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed exceed 0.010 (0,25).
- E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- F. A visual index feature must be located within the cross–hatched area.
- G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- H. Power pin connections should be two or more vias per input, ground and output pin.

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