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APPLICATION NOTE 5507

Understanding the DS1WM Synthesizable 1-Wire Bus Master

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Abstract: Communication with 1-Wire® slave devices requires a 1-Wire master. There are numerous ways to build a 1-Wire master (see reference design 4206, "Choosing the Right 1-Wire Master for Embedded Applications"). This document describes the DS1WM, a synthesizable 1-Wire master that can be implemented in an application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA). The free DS1WM IP is available by request.

Introduction

With the growing popularity and diversity of 1-Wire devices, more engineers are facing the task of how to integrate a 1-Wire master into their systems. Reference design 4206, "Choosing the Right 1-Wire Master for Embedded Applications," describes various options. This document focuses on the DS1WM synthesizable 1-Wire bus master that can be implemented as a function block of an application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA). The DS1WM core uses little chip area (~3470 gates plus two bond pads). It also generates the entire 1-Wire timing by hardware, reducing the initial software development time and cost. Thus the entire application software can be written in high-level language. Besides the 1-Wire communication signal DQ, the DS1WM also provides a control signal STPZ, which assists in meeting the power requirements of certain 1-Wire slaves and allows for large networks with many slaves or extensive cabling. **Figure 1** shows the typical DS1WM application circuit. The DS1WM is available for free in both Verilog and VHDL formats.

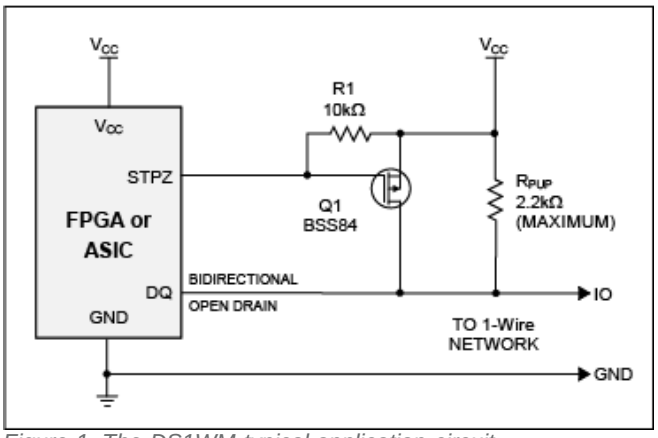

Figure 1. The DS1WM typical application circuit.

Description

Similar to a memory device, the DS1WM connects to the user's system through an 8-bit data bus, using 3 address

lines and the usual control signals (**Figure 2**). An internal divider chain converts any suitable system clock to a 1MHz signal, which in turn controls the 1-Wire timing. The DS1WM supports standard and overdrive 1-Wire communication in single-bit or byte mode, as well as modified timing for long line applications. The host interface and 1-Wire port signals are described in **Table 1**. **Figures 3** to **5** and **Table 2** specify the host interface waveforms and timing.

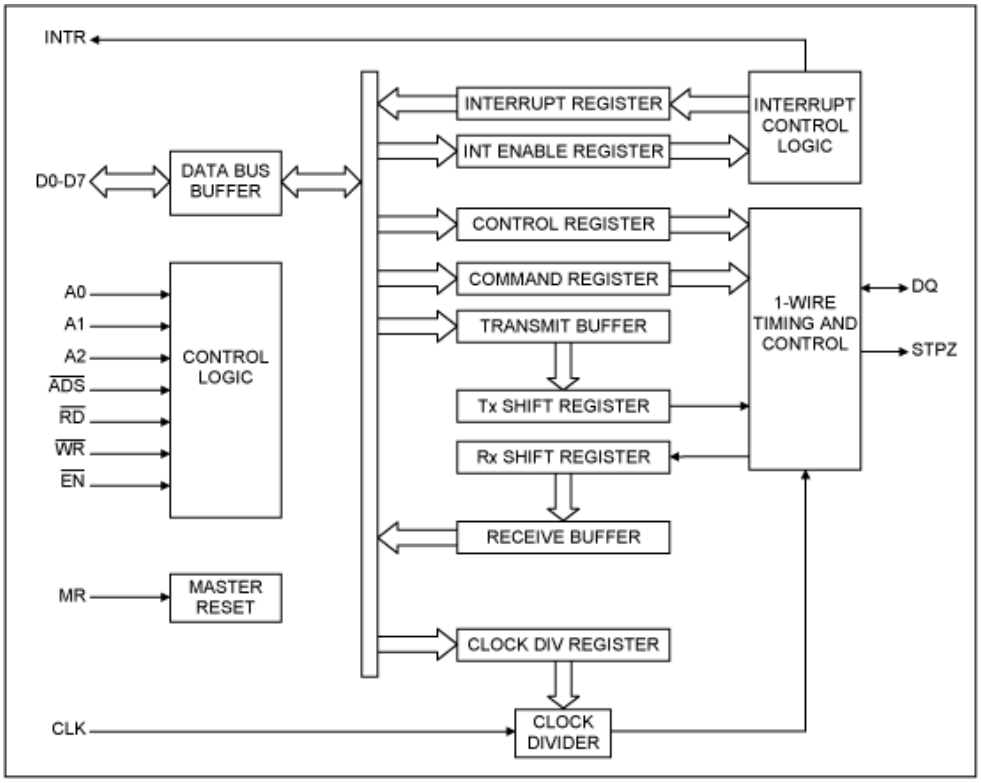

Figure 2. The DS1WM block diagram.

Table 1. Signal Descriptions

Name	Type	Function
MR	I	Master reset. Causes the DS1WM to perform an internal reset with the same result as a power-on reset. MR is not gated by `active-low EN`. The signal is recognized as active by any rising edge on the pin (no minimum duration requirement).
CLK	I	System clock signal. The clock-divider block converts this signal into a ~1.0MHz clock, which in turn controls the 1-Wire timing. The duty cycle should be approximately 50%. See the Clock Divisor Register description for the logically permissible CLK frequencies. The physically permissible upper limit depends on the characteristics of the ASIC/FPGA chosen for implementation.
A[2:0]	I	Address lines of the host interface to access the various memory-mapped device registers. See the Memory Map for register addresses.
`Active-Low ADS`	I	Active-low address strobe of the host interface. The state of the address lines A[2:0] is copied to an internal latch on the rising edge of the address strobe. See the Host Interface Timing diagrams (Figures 3, 4, and 5) for details.
`Active-Low EN`	I	Active-low general enable signal of the host interface. See the Host Interface Timing diagrams (Figures 3, 4, and 5) for details.
D[7:0]	I/O	Bidirectional data bus of the host interface, three-stated. The DS1WM drives these signals during the host read cycle (Figure 3). At all other times, these signals are in a

		high impedance state, allowing the host to communicate with other devices on the data bus.
Active-Low WR	I	Active-low write enable signal of the host interface. The state of the data bus D[7:0] is copied to the addressed register on the rising edge of the active-low WR signal. active-low WR should be inactive (high) unless the host wants to write to the DS1WM. See the Host Interface Timing diagrams (Figures 3 and 5) for details. If both active-low RD and active-low WR are active at the same time, active-low WR dominates.
Active-Low RD	I	Active-low read enable signal of the host interface. When active, the DS1WM puts the contents of the selected register on the data bus for the host to read. Active-low RD should be inactive (high) unless the host wants to read from the DS1WM. See the Host Interface Timing diagram (Figure 4) for details. If both active-low RD and active-low WR are active at the same time, active-low WR dominates.
DQ	I/O	IO driver for the 1-Wire bus. This is an open-drain bidirectional port, which requires a pullup resistor to V_{CC}. For the permissible pullup resistor range, refer to the data sheet of the 1-Wire slaves in the application. The minimum value also depends on the drive characteristics and logic thresholds of the ASIC/FPGA chosen for implementation.
STPZ	O	Active-low control signal for an external P-channel transistor to bypass the pullup resistor at certain times. See the Control Register description, bits STPEN and STP_SPLY, and the STPZ timing diagrams (**Figures 10** to **13**) for details.
INTR	O	Interrupt signal of the host interface. The power-on default polarity is active low, but can be changed to active high through the IAS bit in the Interrupt Enable Register. The INTR signal is inactive unless interrupts are enabled through the Interrupt Enable Register and a qualifying interrupt condition exists. For details see the Interrupt Register description. Reading the Interrupt Register changes the INTR signal to its inactive state.

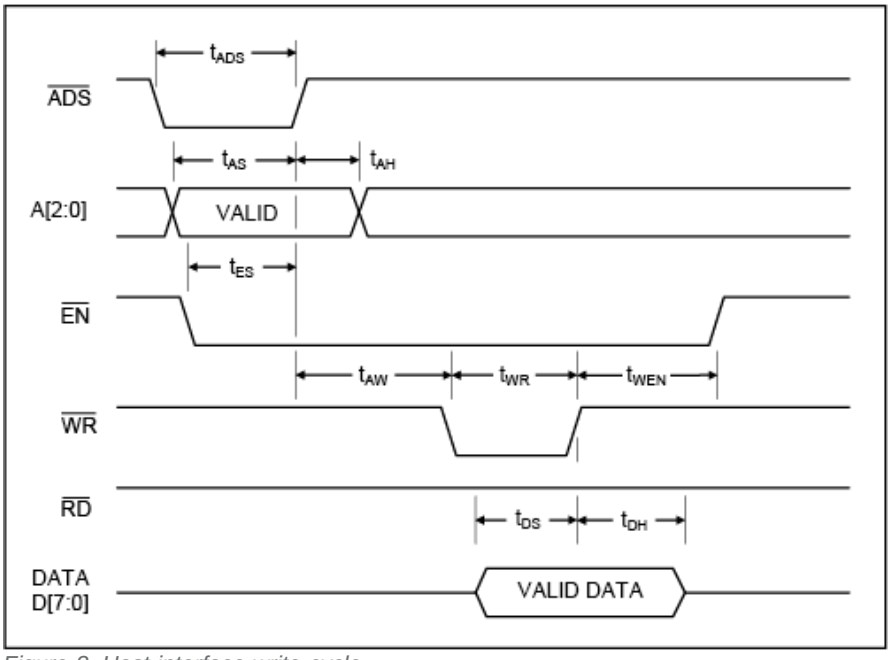

Figure 3. Host interface write cycle.

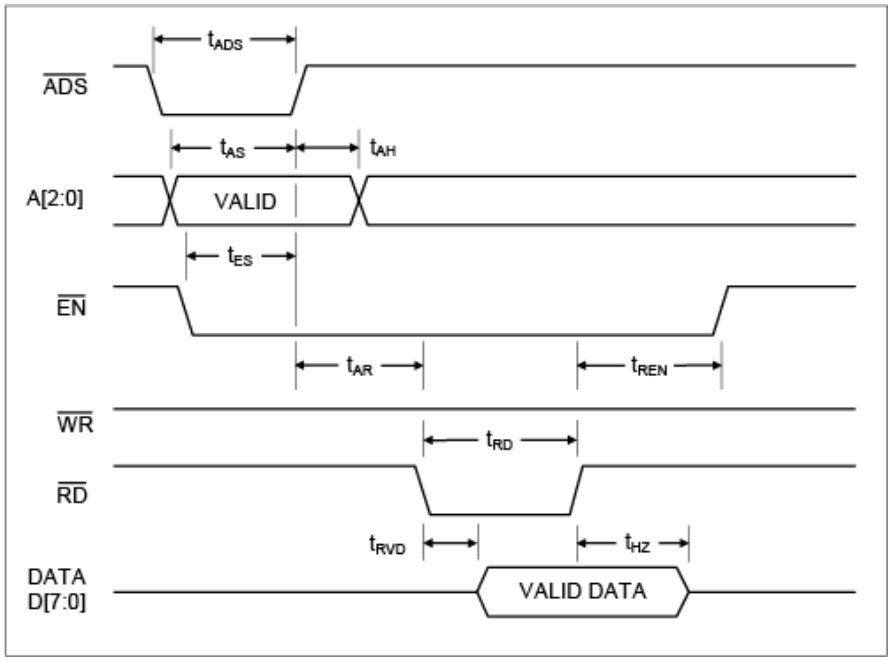

Figure 4. Host interface read cycle.

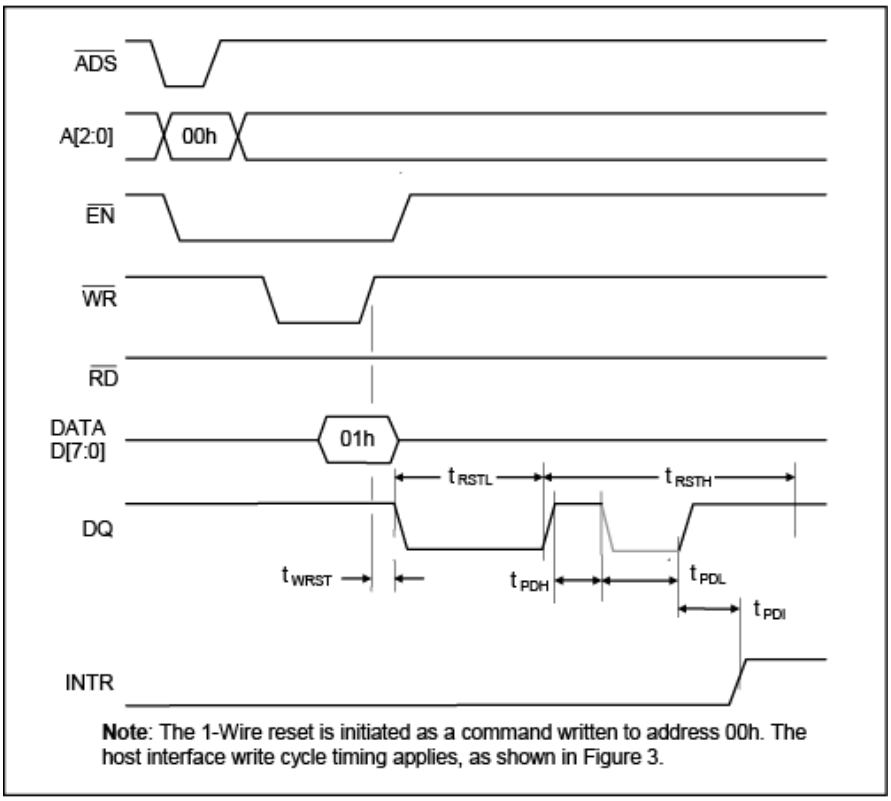

Figure 5. Host interface timing, issuing a 1-Wire Reset.

Table 2. Host Interface Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units

t_{ADS}	Address strobe width	Notes 1, 2	60		ns
t_{AH}	Address hold time	Notes 1, 2	0		ns
t_{AR}	Address latch to read	Notes 1, 2	60		ns
t_{AS}	Address setup time	Notes 1, 2	60		ns
t_{AW}	Address latch to write	Notes 1, 2	60		ns
t_{DH}	Data hold time	Note 1	30		ns
t_{DS}	Data setup time	Note 1	30		ns
t_{ES}	Enable setup time	Note 1	60		ns
t_{HZ}	RD to floating data delay	Note 1	0	100	ns
t_{PDI}	Presence detect to INTR	Note 1	0	100	ns
t_{RD}	RD strobe width	Note 1	125		ns
t_{REN}	Enable hold time from RD	Note 1	20		ns
t_{RVD}	Delay from RD to data	Note 1		60	ns
t_{WEN}	Enable hold time from WR	Note 1	20		ns
t_{WR}	WR strobe width	Note 1	100		ns
t_{WRST}	WR high to reset	Note 1	0	100	ns

Note 1: These values depend on the process used to realize the DS1WM. Values shown are for example purposes only.

Note 2: If `active-low ADS` is tied low, t_{AR} and t_{AW} are measured from t_{ES}. In this case, the falling edge of `active-low RD` or `active-low WR` must occur at least t_{ES} + t_{AR} or t_{ES} + t_{AW} after the falling edge of `active-low EN`.

The host processor communicates with the DS1WM through 6 registers, which are accessed through 3 address lines A[2:0]. **Table 3** shows the memory map.

Table 3. Memory Map

Address	A2	A1	A0	Access	Description
00h	0	0	0	Write/read	Command Register
01h	0	0	1	Write/read	Transmit/Receive Buffer
02h	0	1	0	Read	Interrupt Register
03h	0	1	1	Write/read	Interrupt Enable Register
04h	1	0	0	Write/read	Clock Divisor Register
05h	1	0	1	Write/read	Control Register

Register Descriptions

Command Register

This register is accessed to generate a 1-Wire reset/presence-detect cycle and to activate or deactivate the Search ROM accelerator. In addition to these two functions, the Command Register contains 2 bits to control the DQ pin

directly.

Command Register Bitmap								
ADDR	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
00h	X	X	X	X	OW_IN	FOW	SRA	1WR

This register is read/write. The power-on default is 08h (OW_IN = 1). Bits 4 to 7 have no function; they always read 0 and cannot be set to 1.

Bit Description	Definition	
OW_IN: DQ Input (Read only)	**Purpose**:	Reading the logic state of the DQ pin. Sampling takes place on every falling edge of the CLK signal.
	Code:	1: The voltage at DQ is above V_{IHMIN} (default). 0: The voltage at DQ is below V_{ILMAX}.
	Conditions:	This function is always enabled. OW_IN changes to 1 upon power-on reset or a master reset (MR pin).
	Usage:	In conjunction with FOW to perform 1-Wire communication beyond the 1-Wire Reset and 1-Wire Read/Write functions.
FOW: Force 1-Wire	**Purpose**:	Directly driving the DQ pin under host timing control.
	Code:	1: Activates DQ pulldown 0: Ends DQ pulldown (default)
	Conditions:	This function must be enabled by first writing the EN_FOW bit in the Control Register (address 05h) to 1. Otherwise, FOW has no effect. If both EN_FOW and FOW are 1, the 1-Wire Reset and the 1-Wire Transmit/Receive function (address 01h) have no effect. FOW returns to 0 upon power-on reset or master reset (MR pin). Changing EN_FLOW to 0 has the same effect as writing FOW to 0.
	Usage:	Generating DQ signaling beyond the 1-Wire Reset and 1-Wire Read/Write functions. To read from the 1-Wire bus, change FOW to 0, then wait as needed and read the OW_IN bit. As a safety precaution, if FOW is written to 1 while the STPZ signal is active (low), the STPZ signal immediately changes to inactive (high).
SRA: Search ROM Accelerator	**Purpose**:	Activating the search ROM accelerator.
	Code:	1: The search ROM accelerator is activated. 0: The search ROM accelerator is not activated (default).
	Conditions:	This function is always enabled. SRA returns to 0 upon a power-on reset, a master reset (MR pin), or when written to 0.
	Usage:	The search ROM accelerator saves time when executing the 1-Wire Search algorithm. See the Search Accelerator Operation section for more information.
1WR: 1-Wire Reset	**Purpose**:	Generating a reset/presence detect sequence on the 1-Wire bus.
	Code:	1: A reset/presence detect cycle is in progress. 0: The reset/presence detect cycle is completed (default).
	Conditions:	This function is always enabled. 1WR returns to 0 upon a power-on reset, a master reset (MR pin) or the completion of the 1-Wire reset/presence detect cycle. A 1-Wire reset/presence-detect cycle can be aborted by writing this bit to 0.
	Usage:	Writing this bit to 1 starts a 1-Wire reset/presence detect cycle and affects the PD and PDR bits in the Interrupt Register (address 02h).

Transmit/Receive Buffer

This is the location to which the host processor writes a data byte to be transmitted on the 1-Wire bus. If the 1-Wire slave is in a state to respond with data, the host writes a byte FFh to this register and then, after the byte is transmitted, reads this register again to retrieve that data sent by the 1-Wire slave.

Transmit/Receive Buffer Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
01h	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

This register is read/write. The power-on default is 00h.

Bit Description	Definition	
Data[7:0]: Transmit/Receive Data	**Purpose**:	Providing data for transmission on the 1-Wire bus; accessing data received from 1-Wire bus.
	Code:	N/A
	Conditions:	1-Wire communication can be performed in bit mode or in byte mode (default). In bit mode, only Data0 is relevant. Bit mode is selected by writing the BIT_CTL bit in the Control Register (address 05h) to 1. Data[7:0] returns to 00h upon a power-on reset or a master reset (MR pin).
	Usage:	General 1-Wire communication except for 1-Wire reset. The 1-Wire speed is selected by the OD bit in the Control Register (address 05h).

Interrupt Register

This register provides access to flags from current status, transmit, receive, and 1-Wire reset operations. All of these flags can generate an interrupt on the INTR pin if the corresponding enable bit is set in the Interrupt Enable Register. To clear the INTR signal, the Interrupt Register must be read. Reading the Interrupt Register always sets the INTR pin inactive even if not all flags are cleared.

Interrupt Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
02h	OW_LOW	OW_SHORT	RSRF	RBF	TEMT	TBE	PDR	PD

This register is read only. The power-on default is 0Eh (TEMT, TBE, PDR = 1, PD = 0).

Bit Description	Definition	
OW_LOW: 1-Wire Event	**Purpose**:	Signaling the arrival of a slave on the 1-Wire bus.
	Code:	1: A slave has arrived. 0: No slave arrival since the last reading of the Interrupt Register (default).
	Conditions:	This function is always enabled. OW_LOW returns to 0 upon reading the Interrupt Register, a power-on reset or a master reset (MR pin).
	Usage:	A slave arriving on the idle bus (= no communication) generates a spontaneous presence pulse, which sets this bit. A short circuit on the idle bus also sets this bit.
OW_SHORT: 1-Wire Shorted	**Purpose**:	Signaling a short circuit on the 1-Wire bus.
	Code:	1: The 1-Wire bus is shorted. 0: The 1-Wire bus is in normal operating conditions (default).
	Conditions:	This function is always enabled. OW_SHORT returns to 0 upon reading the Interrupt Register, a power-on reset or a master reset (MR pin).

	Usage:	Prior to generating a 1-Wire reset or time slot, the DS1WM checks whether the 1-Wire bus is idle high. If the bus is low at that time, no communication can take place. This situation is signaled as a short circuit.
RSRF: Receive Shift Register Full	**Purpose**:	Signaling the status of the Receive Shift Register.
	Code:	1: The Receive Shift Register is full. 0: The Receive Shift Register is empty or receiving data (default).
	Conditions:	This function is always enabled. RSRF returns to 0 when the Receive Shift Register content is transferred to the Receive Buffer (address 01h) for the host to read, upon power-on reset, or a master reset (MR pin).
	Usage:	When the RSRF gets set and the RBF is not set (i.e., meaning the Receive Shift Register is full and the Receive Buffer flag is clear), the transfer takes place on the rising edge of the internal 1MHz clock.
RBF: Receive Buffer Full	**Purpose**:	Signaling the status of the Receive Buffer.
	Code:	1: There is new data in the Receive Buffer. 0: There is no new data in the Receive Buffer (default).
	Conditions:	This function is always enabled. RBF returns to 0 upon reading the Receive Buffer (address 01h), a power-on reset, or a master reset (MR pin). Reading the Interrupt Register without first having read the Receive Buffer triggers another interrupt if ERBF = 1 & RBF = 1.
	Usage:	Normal communication with 1-Wire slaves. If not using interrupts, poll the Interrupt Register to detect events. If using the RBF interrupt (ERBF = 1), read the Receive Buffer prior to reading the Interrupt Register.
	The process to use the RBF flag looks like this: 1. Write FF to the TX buffer and enable the TBE flag. 2. Wait for the interrupt pin to trigger. 3. When the interrupt occurs, read the interrupt register and confirm TBE set. 4. Clear ETBE bit and now set the ETMT bit. 5. Wait for the interrupt pin to trigger. 6. When the interrupt occurs, read the interrupt register and confirm ETMT set. 7. Clear the ETMT bit and now set the ERBF bit. 8. Wait for the interrupt pin to trigger. 9. When the interrupt occurs, read the interrupt register and confirm RBF set. 10. Read the RX Buffer. 11. Clear the ERBF after reading the RX Buffer.	
TEMT: Transmit Shift Register Empty	**Purpose**:	Signaling the status of the Transmit Shift Register.
	Code:	1: The Transmit Shift Register is empty, ready for new data (default). 0: The Transmit Shift Register is busy sending data.
	Conditions:	This function is always enabled. TEMT returns to 0 when the Transmit Buffer content (address 01h) is transferred to the Transmit Shift Register. TEMT changes to 1 upon power-on reset or a master reset (MR pin).
	Usage:	The transfer takes place on the internal 1MHz clock as soon as the TBE is set.
TBE: Transmit Buffer Empty	**Purpose**:	Signaling the status of the Transmit Buffer.
	Code:	1: The Transmit Buffer is empty, ready for new data (default). 0: The Transmit Buffer is waiting for the Transmit Shift Register to finish sending data.
	Conditions:	This function is always enabled. TBE returns to 0 upon writing to Transmit Buffer (address 01h). TBE changes to 1 upon power-on reset or a master reset (MR pin).
	Usage:	Normal communication with 1-Wire slaves.

PDR: Presence Detect Result	**Purpose**:	Signaling the result of the presence detect cycle.
	Code:	1: No presence pulse was detected (default). 0: A presence pulse was detected.
	Conditions:	This function is always enabled. PDR changes to 1 upon power-on reset or a master reset (MR pin) or if no presence is detected.
	Usage:	Normal communication with 1-Wire slaves.
PD: Presence Detect	**Purpose**:	Signaling the completion of a 1-Wire reset/presence detect cycle.
	Code:	1: The most recent reset/presence detect is completed. 0: There was no reset/presence detect cycle since last reading the Interrupt Register (default).
	Conditions:	This function is always enabled. PD returns to 0 upon reading the Interrupt Register, a power-on reset or a master reset (MR pin).
	Usage:	Normal communication with 1-Wire slaves.

Interrupt Enable Register

The Interrupt Enable Register allows the system programmer to specify the source of interrupts which will cause the INTR pin to be active, and to define the active state for the INTR pin. When a Master Reset is received all bits in this register are cleared to 0 disabling all interrupt sources and setting the active state of the INTR pin to LOW. The INTR pin is reset to an inactive state by reading the Interrupt Register.

Interrupt Enable Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
03h	EOWL	EOWSH	ERSF	ERBF	ETMT	ETBE	IAS	EPD

This register is read/write only. The power-on default is 00h.

Bit Description	Definition	
EOWL: Enable 1-Wire Low Interrupt	**Purpose**:	Enabling the interrupt upon arrival of a slave on the 1-Wire bus.
	Code:	1: The OW_LOW interrupt is enabled. 0: The OW_LOW interrupt is disabled (default).
	Conditions:	None. EOWL returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	This interrupt is useful in applications where 1-Wire slaves come and go, e. g., access control using ¡Button® devices as keys.
EOWSH: Enable 1-Wire Short Interrupt	**Purpose**:	Enabling the interrupt upon a short circuit of the 1-Wire bus.
	Code:	1: The OW_SHORT interrupt is enabled. 0: The OW_SHORT interrupt is disabled (default).
	Conditions:	None. EOWSH returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	This interrupt is useful in access control applications, alarming the host processor of potential tampering or sabotage.
ERSF: Enable Receive Shift Register Full Interrupt	**Purpose**:	Enabling the interrupt upon the Receive Shift Register Full condition.
	Code:	1: The RSRF interrupt is enabled. 0: The RSRF interrupt is disabled (default).
	Conditions:	None. ERSF returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	This interrupt can be used to ensure that you don't have data in both the RX Buffer and the RX Shift Register. If both do have data you need to read twice to

		clear out the buffer.
ERBF: Enable Receive Buffer Full Interrupt	**Purpose**: **Code**: **Conditions**: **Usage**:	Enabling the interrupt upon the Receive Buffer Full condition. 1: The RBF interrupt is enabled. 0: The RBF interrupt is disabled (default). None. ERBF returns to 0 upon power-on reset or a master reset (MR pin). This interrupt is useful during 1-Wire communication, informing the host processor that the receive buffer has data ready for reading.
ETMT: Enable Transmit Shift Register Empty Interrupt	**Purpose**: **Code**: **Conditions**: **Usage**:	Enabling the interrupt upon the Transmit Shift Register Empty condition. 1: The TEMT interrupt is enabled. 0: The TEMT interrupt is disabled (default). None. ETMT returns to 0 upon power-on reset or a master reset (MR pin). This interrupt is useful to know when the 1-Wire wire bits are all transmitted.
ETBE: Enable Transmit Buffer Empty Interrupt	**Purpose**: **Code**: **Conditions**: **Usage**:	Enabling the interrupt upon the Transmit Buffer Empty condition. 1: The TBE interrupt is enabled. 0: The TBE interrupt is disabled (default). None. ETBE returns to 0 upon power-on reset or a master reset (MR pin). This interrupt is useful during 1-Wire communication, informing the host processor that the transmit buffer is empty, ready for new data.
IAS: INTR Active State	**Purpose**: **Code**: **Conditions**: **Usage**:	Setting the active state polarity of the INTR signal 1: The INTR polarity is active high. 0: The INTR polarity is active low (default). None. IAS returns to 0 upon power-on reset or a master reset (MR pin). If the INTR signal is used, this bit matches the signal polarity to the host processor's needs.
EPD: Enable Presence Detect Interrupt	**Purpose**: **Code**: **Conditions**: **Usage**:	Enabling the interrupt upon the completion of a 1-Wire reset/presence detect cycle. 1: The PD interrupt is enabled. 0: The PD interrupt is disabled (default). None. EPD returns to 0 upon power-on reset or a master reset (MR pin). This interrupt is useful during 1-Wire communication, informing the host processor that the 1-Wire reset/presence detect (PD) cycle is completed and that the result is found in the PDR bit of the Interrupt Register (address 02h). EPD is to be enabled it before the 1-Wire reset/PD cycle. Then you wait for the interrupt and when the interrupt occurs you read to confirm PD was the cause.

Clock Divisor Register

The 1-Wire timing requires a 1MHz internal clock. The DS1WM generates this clock frequency from an external reference on the CLK pin. The external clock should have a 50% duty cycle is preferred. The Clock Divisor Register lets the host processor control a clock divider and prescaler to get from the external CLK signal as close as possible to the 1MHz needed for 1-Wire timing. The clock divisor must be configured before communication on the 1-Wire bus can take place. If using an FPGA, it is recommended to replace the clock-divider block with FPGA clock resources to generate the 1MHz internal clock. This avoids gated clocks in the FPGA.

Clock Divisor Register Bitmap								
ADDR	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**

04h	CLK_EN	X	X	DIV2	DIV1	DIV0	PRE1	PRE0

This register is read/write. The power-on default is 00h. Bits 5 and 6 have no function; they always read 0 and cannot be set to 1.

Bit Description	Definition	
CLK_EN: Enable 1-Wire Timing System	**Purpose**:	Enabling the circuit that controls the 1-Wire timing.
	Code:	1: The 1-Wire timing system is enabled. 0: The 1-Wire timing system is disabled (default).
	Conditions:	CLK_EN returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	As a precondition for 1-Wire communication, this bit must be written to 1. To save power at times without 1-Wire communication, this bit can be changed to 0.
DIV[2:0]: Binary Divider Ratio	**Purpose**:	Configuring the binary divider to generate, together with the prescaler, a 1µs clock that governs the entire 1-Wire timing.
	Code:	000b: Divide by 1 (pass through, default) 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 110b: Divide by 64 111b: Divide by 128
	Conditions:	DIV[2:0] returns to 000b upon power-on reset or a master reset (MR pin).
	Usage:	As a precondition for 1-Wire communication, these bits must be written to the appropriate value, which depends on the available master clock frequency. See **Table 4** for guidance.
PRE[1:0]: Prescaler Ratio	**Purpose**:	Configuring the prescaler to generate, together with the binary divider, a 1µs clock that governs the entire 1-Wire timing.
	Code:	00b: Divide by 1 (pass through, default) 01b: Divide by 3 10b: Divide by 5 11b: Divide by 7
	Conditions:	PRE[1:0] returns to 00b upon power-on reset or a master reset (MR pin).
	Usage:	As a precondition for 1-Wire communication, these bits must be written to the appropriate value, which depends on the available master clock frequency. See Table 4 for guidance.

Table 4. Clock Divisor Register Settings

Min CLK Frequency (MHz)	Max CLK Frequency (MHz)	Max CLK Error (%)	Overall Divider Ratio	DIV2	DIV1	DIV0	PRE1	PRE0
1	1.25	25	1	0	0	0	0	0
2	2.5	25	2	0	0	1	0	0
3	3.75	25	3	0	0	0	0	1

4	< 5	25	4	0	1	0	0	0
5	< 6	20	5	0	0	0	1	0
6	< 7	17	6	0	0	1	0	1
7	< 8	14	7	0	0	0	1	1
8	< 10	25	8	0	1	1	0	0
10	< 12	20	10	0	0	1	1	0
12	< 14	17	12	0	1	0	0	1
14	< 16	14	14	0	0	1	1	1
16	< 20	25	16	1	0	0	0	0
20	< 24	20	20	0	1	0	1	0
24	< 28	17	24	0	1	1	0	1
28	< 32	14	28	0	1	0	1	1
32	< 40	25	32	1	0	1	0	0
40	< 48	20	40	0	1	1	1	0
48	< 56	17	48	1	0	0	0	1
56	< 64	14	56	0	1	1	1	1
64	< 80	25	64	1	1	0	0	0
80	< 96	20	80	1	0	0	1	0
96	< 112	17	96	1	0	1	0	1
112	< 128	14	112	1	0	0	1	1
128	< 160	25	128	1	1	1	0	0
160	< 192	20	160	1	0	1	1	0
192	< 224	17	192	1	1	0	0	1
224	280	25	224	1	0	1	1	1
320	< 384	20	320	1	1	0	1	0
384	< 448	17	384	1	1	1	0	1
448	560	25	448	1	1	0	1	1
640	800	25	640	1	1	1	1	0
896	1120	25	896	1	1	1	1	1

Example: If the system clock frequency is 15MHz, the closest overall divider ratio to reach 1MHz is 14. This corresponds to a value of 87h to be written to the Clock Divisor Register. The clock error in this case is (15/14) -1, or 7%.

Control Register

The host processor accesses this register to select the desired operating mode of the DS1WM. These modes include 1-Wire power delivery, recharge accelerator, single bit mode vs. byte mode, long line mode, and presence pulse masking. Correct use of these functions increases the data integrity on the 1-Wire bus.

Control Register Bitmap								
ADDR	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
05h	X	OD	BIT_CTL	STP_SPLY	STPEN	EN_FOW	PPM	LLM

This register is read/write. The power-on default is 00h. Bit 7 has no function; it always reads 0 and cannot be set to 1.

Bit Description	Definition	
OD: 1-Wire Speed	**Purpose**:	Selecting the speed to be used for 1-Wire communication.
	Code:	1: Overdrive speed is selected. 0: Standard speed is selected (default).
	Conditions:	None. OD returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	With most 1-Wire slaves, the power-on default is standard speed. With those parts, the speed change to overdrive requires that the 1-Wire slaves first receive the appropriate switching command at standard speed. After that, the OD bit of the DS1WM must be changed to 1. To switch back to standard speed, change the OD bit to 0 and issue a 1-Wire reset (see Command Register, address 00h).
BIT_CTL: Bit Control	**Purpose**:	Selecting bit mode or byte mode for 1-Wire communication.
	Code:	1: The DS1WM operates in bit mode. 0: The DS1WM operates in byte mode (default).
	Conditions:	None. BIT_CTL returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	Most 1-Wire communication occurs in byte mode (power-on default). If bit mode is selected, only the least significant bit in the Transmit/Receive buffer is used/valid. Consequently, the corresponding full/empty bits in the Interrupt Register (address 02h) are set after 1 time slot rather than 8 time slots in byte mode.
STP_SPLY: Strong Pullup Power Delivery	**Purpose**:	Activating the strong pullup power delivery function. This function uses the STPZ pin to control a p-channel transistor to bypass the 1-wire pullup resistor.
	Code:	1: The strong pullup power delivery is activated. 0: The strong pullup power delivery is not activated (default).
	Conditions:	This function must be enabled by first writing the STPEN bit in the Control Register to 1. STP_SPLY returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	Some 1-Wire slaves need extra power, e.g., to program EEPROM, measure temperature or perform numeric calculations. Depending on the operating environment, the 1-Wire pullup resistor must be bypassed to maintain the minimum voltage required by the slave to function properly. The host processor must set STP_SPLY to 1 before the slave's high current demand begins and should write STP_SPLY to 0 after the high current phase has ended.
STPEN: Active Pullup Enable	**Purpose**:	Enabling active pullup to minimize the rise time on a heavily loaded 1-Wire bus. This function uses the STPZ pin to control a p-channel transistor to *temporarily* bypass the 1-wire pullup resistor.
	Code:	1: The active pullup is enabled. 0: The active pullup is disabled (default).
	Conditions:	None. STPEN returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	Since it improves the power supply situation of parasitically powered 1-Wire slaves, active pullup should always be enabled. Active pullup must be enabled when operating the 1-Wire bus near the minimum permissible pullup voltage, or

		with a long bus cable or with multiple slave devices. After a power-on reset, the active pullup is disabled. See **Table 6**, STPZ Timing Specification, for details.
EN_FOW: Enable Force 1-Wire	**Purpose**:	Enabling the Force 1-Wire command.
	Code:	1: The Force 1-Wire command is enabled. 0: The Force 1-Wire command is disabled (default).
	Conditions:	None. EN_FOW returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	Generating DQ signals beyond 1-Wire Reset and 1-Wire read/write functions. For more details, see the FOW bit description of the Command Register (address 00h).
PPM: Presence Pulse Masking	**Purpose**:	Pre-empting the presence pulse generated by 1-Wire slaves.
	Code:	1: Presence pulse masking is enabled. 0: Presence pulse masking is disabled (default).
	Conditions:	None. PPM returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	In a long-line environment, presence pulses generated by 1-Wire slaves can cause ringing on the bus. Presence pulse masking can prevent adverse effects caused by the presence pulse. If PPM is 1, the presence detect result (PDR bit of the Interrupt Register, address 02h) is always 0, even if the is no 1-Wire slave on the bus. See **Table 5**, DQ Signal Timing Specification, for details.
LLM: Long Line Mode	**Purpose**:	Modifying the standard speed timing to be more adequate for a long line application environment.
	Code:	1: Long line mode is enabled. 0: Long line mode is disabled (default).
	Conditions:	None. LLM returns to 0 upon power-on reset or a master reset (MR pin).
	Usage:	Long line mode changes the Write 1 low time, data sampling time, and recovery time. See Table 5, DQ Signal Timing Specification, for details.

1-Wire Port Description

The 1-Wire port uses the signals DQ and STPZ. The 1-Wire communication takes place on DQ. The DS1WM supports the following 1-Wire communication waveforms: reset/presence-detect cycle, write-zero time slot, write-one time slot, and read-data time slot.

Reset/Presence-Detect Cycle

This signal (**Figure 6**) consists of two elements: the DS1WM pulldown during the reset-low time t_{RSTL}, and the t_{RSTH} window during which, after a delay of t_{PDH}, a 1-Wire slave pulls the line low for t_{PDL} to signal its presence. To test for a presence pulse, the DS1WM first waits for t_{PDW} and then during t_{PDSW} samples the voltage on DQ. Note that the DS1WM does not control the duration of t_{PDH} and t_{PDL}.

The DS1WM can be configured to mask the presence generated by slaves (see Control Register, bit PPM). If the PPM bit is 1, the DS1WM generates a presence pulse (dotted line) that begins as t_{PPMS} and lasts until t_{PPME}.

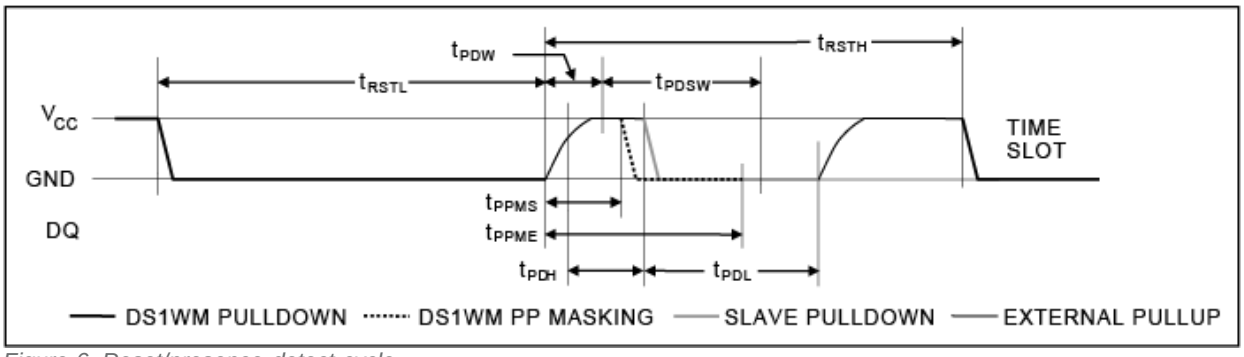

Figure 6. Reset/presence detect cycle.

Write-Zero Time Slot

This time slot (**Figure 7**) consists of two elements: the DS1WM pulldown as specified by t_{W0L} and the recovery time t_{REC0}. The sum of t_{W0L} and t_{REC0} is identical to t_{SLOT}.

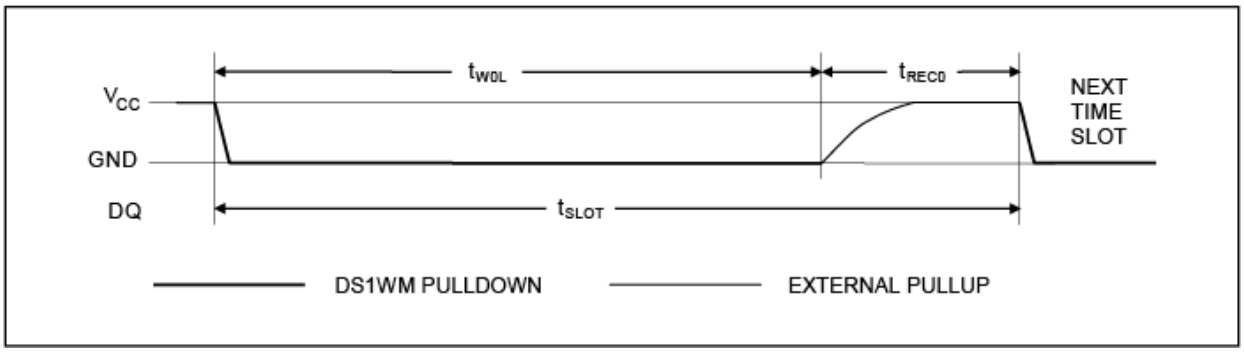

Figure 7. Write-zero time slot.

Write-One Time Slot

This time slot (**Figure 8**) consists of two elements: the DS1WM pulldown as specified by t_{W1L} and the remainder of the time slot.

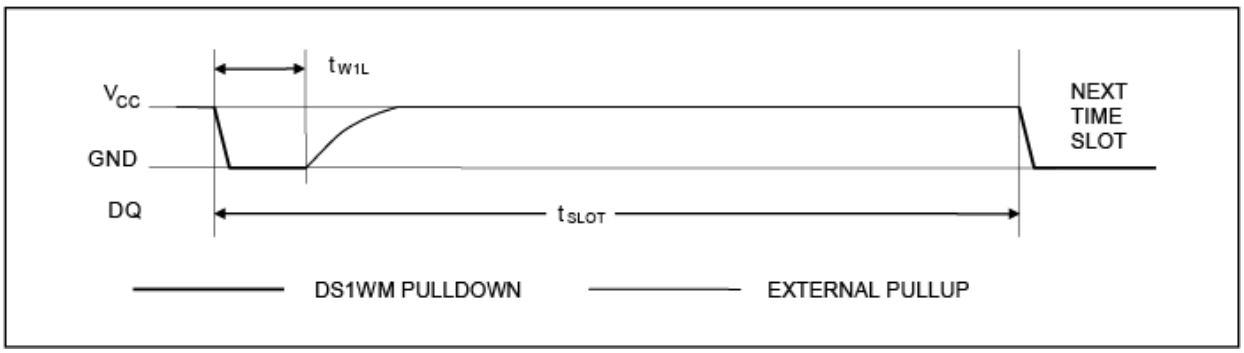

Figure 8. Write-one time slot.

Read-Data Time Slot

This time slot (**Figure 9**) consists of three elements: the DS1WM pulldown as specified by t_{W1L}; the slave pulldown time; and the remainder of the time slot. At t_{MSR}, the DS1WM samples the voltage on DQ. Note that a 1-Wire slave, when responding with a zero, starts pulling the DQ line low before t_{W1L} is expired.

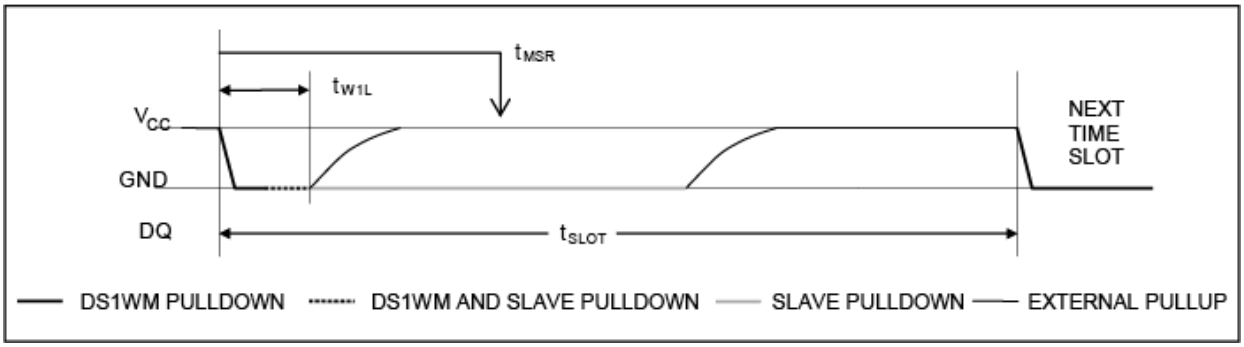

Figure 9. Read-data time slot.

Table 5. DQ Signal Timing Specifications (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
τ	Time base period	(Note 2)	0.8	1	µs
t_{SLOT}	Time-slot duration	Standard speed, LLM = 0	56	70	µs
		Standard speed, LLM = 1	64	80	
		Overdrive speed	8	10	
t_{W0L}	Write-zero low time	Standard speed	48	60	µs
		Overdrive speed	6.4	8	
t_{W1L}	Write-one/read low time	Standard speed, LLM = 0	4.8	6	µs
		Standard speed, LLM = 1	6.4	8	
		Overdrive speed	0.8	1	
t_{MSR}	Read sample time	Standard speed, LLM = 0	12	15	µs
		Standard speed, LLM = 1	19.2	24	
		Overdrive speed	1.6	2	
t_{REC0}	Write-zero recovery time	Standard speed, LLM = 0	8	10	µs
		Standard speed, LLM = 1	16	20	
		Overdrive speed	1.6	2	
t_{RSTL}	Reset low time	Standard speed	480	600	µs
		Overdrive speed	56	70	
t_{RSTH}	Reset high time	Standard speed	384	480	µs
		Overdrive speed	46.4	58	
t_{PDW}	Presence-detect wait time	Standard speed, LLM = 0	8	10	µs
		Standard speed, LLM = 1	8	10	
		Overdrive speed	1.6	2	
t_{PDSW}	Presence-detect sample window	Standard speed, LLM = 0	48.8	61	µs
		Standard speed, LLM = 1	60.8	76	
		Overdrive speed	6.4	8	

t_{PPMS}	Presence-pulse mask START	Standard speed only	16	20	µs
t_{PPME}	Presence-pulse mask end	Standard speed only	72	90	µs

Note 1: The timing values depend on the internal logic. If the I/O drivers are slow, these times will change accordingly.

Note 2: System Clock CLK input frequency and Clock Divisor Settings according to Table 4.

STPZ Timing

If enabled (see Control Register, STPEN bit), the STPZ signal activates an external p-channel transistor at certain times to speed up the recharge of the 1-Wire bus. This function is generally needed at overdrive speed and with larger networks at standard speed. Figures 10 and 11 show the STPZ signal for the reset/presence-detect cycle and communication waveforms.

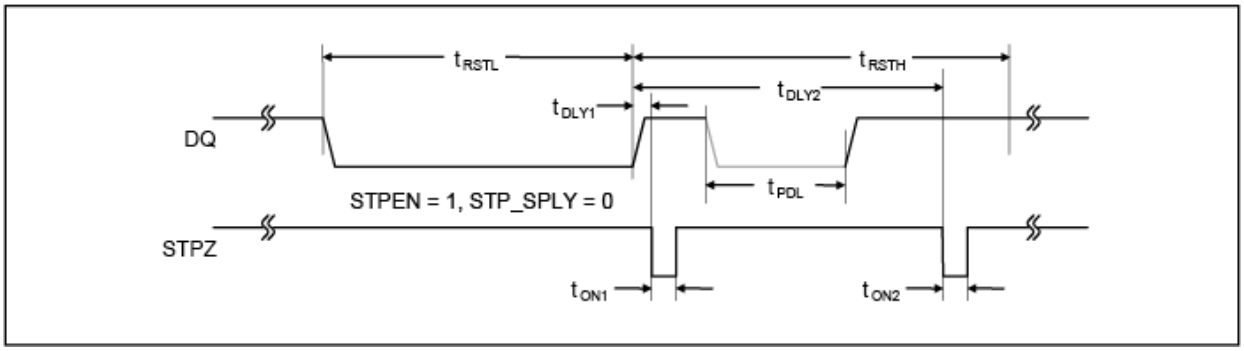

Figure 10. STPZ timing during the reset/presence detect cycle.

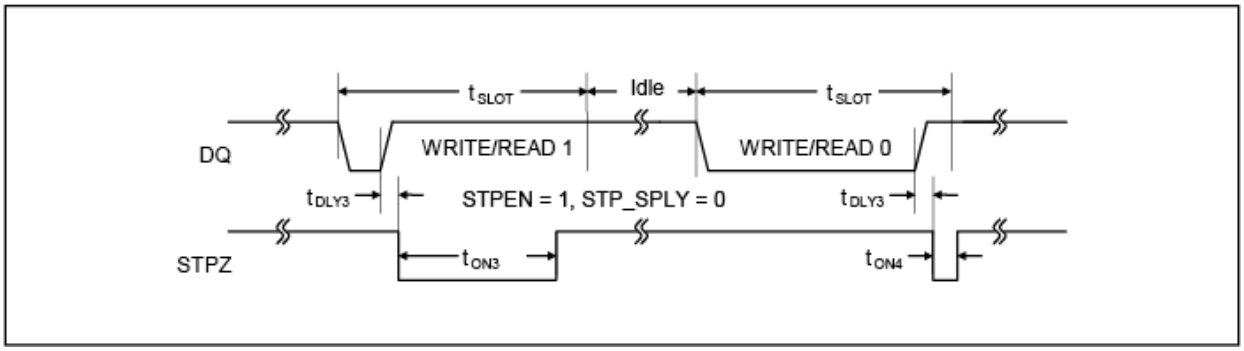

Figure 11. STPZ timing during read/write time slots.

Several 1-Wire slaves need extra power at certain times during the communication protocol. The extra power-supply delivery function is enabled through the STP_SPLY bit in the Control Register. If both STPEN and STP_SPLY are enabled, the STPZ signal remains active (low) whenever possible (see Figures 12 and 13).

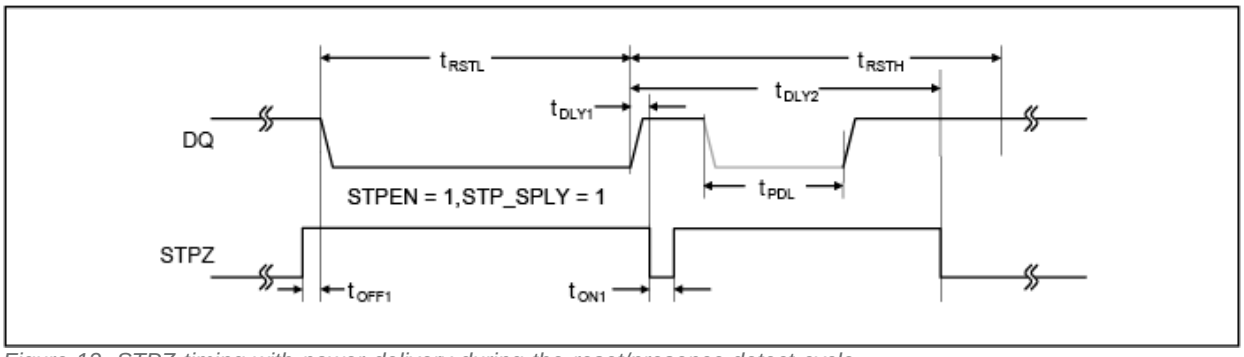

Figure 12. STPZ timing with power delivery during the reset/presence detect cycle.

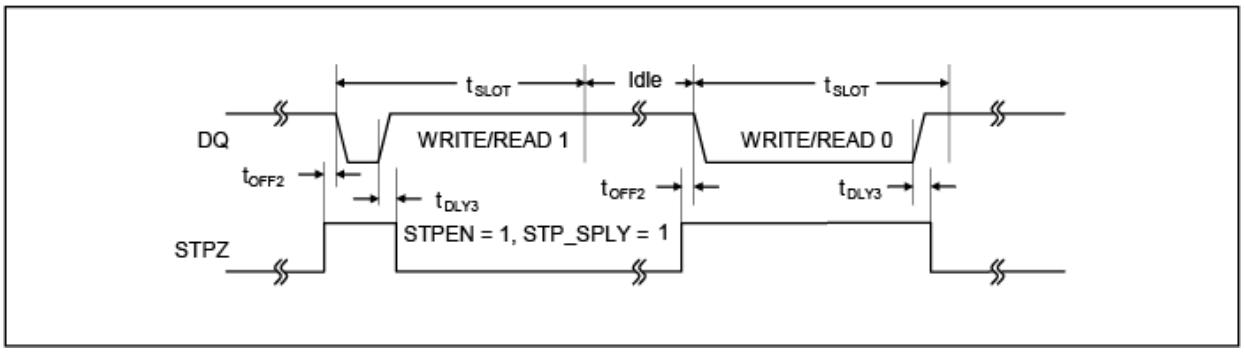

Figure 13. STPZ timing with power delivery during read/write time slots.

Table 6. STPZ Timing Specifications (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{ON1}	Active time for presence detect	Standard speed	6.4	8	µs
		Overdrive speed	0.8	1	
t_{ON2}	Active time for presence detect recovery		8	10	µs
t_{ON3}	Active time for write-one recovery (Notes 2, 3)	Standard speed	51.2	64	µs
		Overdrive speed	7.2	9	
t_{ON4}	Active time for write-zero recovery (Notes 2, 3)	Standard speed	6.4	8	µs
		Overdrive speed	0.8	1	
t_{DLY1}	Delay time for presence detect		0.8	1	µs
t_{DLY2}	Delay time for presence detect recovery (Note 4)	Standard speed	399.2	499	µs
		Overdrive speed	31.2	39	
t_{DLY3}	Delay time for write-one and write-zero recovery		0.8	1	µs
t_{OFF1}	Turn-off time for 1-Wire Reset		1.6	2	µs
t_{OFF2}	Turn-off time for write-one and write-zero	(Note 5)	0.8	1	µs

Note 1: The timing values depend on the internal logic. If the I/O drivers are slow, these times will change accordingly.

Note 2: There is no timing difference for sending out and receiving bits within a byte. The difference comes when the last bit of the byte is finished being sent out. At this point, the signal is either enabled continuously until the next reset or time slot begins, or enabled only for t_{ON3} or t_{ON4}.

Note 3: When performing a read versus a write time slot, the master provides the same active time for write-one and write-zero. However, the input from the DQ line is sensed every 1µs for a high value. If DQ is high, the STPZ signal is enabled. If the DQ line is low, the STPZ signal remains disabled until the high is sensed. In all write time slots, a high is sensed immediately.

Note 4: This parameter is the time delay until the master begins to monitor the DQ input level. If the line is already high, then STPZ will be enabled. If not, it will wait to enable STPZ until the next state machine clock after the DQ line has recovered.

Note 5: The very first bit in a byte transmission has an extended t_{OFF2} of 4µs due to the order of states the master's state machine runs through.

Device Operation

After power-on, the host first accesses the Clock Divisor Register to write the appropriate values for the prescaler and divider and to enable the 1-Wire timing system. If the application uses the STPZ output, the STPEN bit in the Control Register must be set. If the application uses the INTR signal, the host writes to the Interrupt Enable Register to define the INTR active state polarity and to select the conditions under which the INTR signal is to be activated. This concludes the setup phase. Now the DS1WM is ready to operate at standard speed and in byte mode.

Generating a 1-Wire Reset/Presence-Detect Cycle

The host writes the code 01h to the Command Register. If the Presence Detect Interrupt is enabled (EPD bit), the host could perform other tasks while the DS1WM is busy with the reset/presence-detect cycle. After the cycle is completed, the host reads the Interrupt Register (PDR bit) to see whether a presence pulse was detected.

Writing a Byte to the 1-Wire Line

To send a byte on the 1-Wire bus, the user writes the desired data to the Transmit Buffer. The data is then moved to the Transmit Shift Register where it is shifted serially onto the bus LSB first. A new byte of data can then be written to the Transmit Buffer. As soon as the Transmit Shift Register is empty, the data will be transferred from the Transmit Buffer and the process repeats. Each of these registers has a flag that may be used as an interrupt source. The Transmit Buffer Empty (TBE) flag is set when the Transmit Buffer is empty and ready to accept a new byte. As soon as a byte is written into the Transmit Buffer, TBE is cleared. The Transmit Shift Register Empty (TEMT) flag is set when the Shift Register has no data in it and is ready to accept a new byte. As soon as a byte of data is transferred from the Transmit Buffer, TEMT is cleared and TBE is set.

Reading a Byte from the 1-Wire Line

To read data from the 1-Wire bus, a slave device must first be ready to transmit depending on commands already received from the DS1WM. Reading from the 1-Wire line is similar to writing. The host initiates a read by writing an FFh byte to the Transmit Buffer. The wired-AND of the written data and the data from the slave device is then shifted into the Receive Shift Register. When the Receive Shift Register is full, the data is transferred to the Receive Buffer, where it can be accessed by the host. If the slave device is not ready to transmit, the data received is identical to that transmitted. The Receive Buffer Register can also generate interrupts. The Receive Buffer flag (RBF) is set when data is transferred from the Receive Shift Register and cleared when the host reads the register. If RBF is set, no further transmissions should be made on the 1-Wire bus or else data may be lost, as the byte in the Receive Buffer will be overwritten by the next received byte.

1-Wire Communication in Bit Mode

To activate the bit mode, the host writes the BIT_CTL bit in the Control Register to 1. Subsequent communication between host and DS1WM is the same as in byte mode. However, only the least significant bit in the transmit/receive buffer is relevant.

Changing Between Standard and Overdrive Speed

To switch between 1-Wire speeds, the host writes the OD bit in the Control Register to 1 (overdrive) or to 0 (standard). Any 1-Wire communication after updating the OD bit takes place at the new speed. Long line mode (LLM bit) is a variant of standard speed.

Meeting Slave Extra Power Requirements

The 1-Wire slave data sheets specify when, during a function command, extra power is required. To accommodate such a slave, the host operates the DS1WM using reset, byte, or bit functions to get the slave close to the state where the extra power is needed. Then the host sets both the STPEN and the STP_SPLY bits in the Control Register. Next the host performs the byte or bit read/write operation, after which the slave needs extra power. Then the host waits until the high-power phase is over and accesses the Control Register again to write the STP_SPLY bit to 0. The STPEN bit can remain set. The power delivery function works only if the STPZ pin is connected to a transistor, as shown in Figure 1.

Search Accelerator Operation

Application note 187, "1-Wire Search Algorithm," explains how the Search ROM function works. The search accelerator is a feature that minimizes the communication between host and DS1WM when performing a 1-Wire search. The search accelerator of the DS1WM is identical to the accelerator in the DS2480B. Therefore, the search fundamentals of application note 192, "Using the DS2480B Serial 1-Wire Line Driver" ("OWSearch" section), are also valid for the DS1WM. Of course, the DS2480B-specific command and echo bytes do not apply here.

Before the search accelerator can be used, a 1-Wire reset/presence-detect cycle must have been performed and the Search ROM command (F0h) must have been sent out in byte mode. Now the search accelerator is activated by writing the SRA bit in the Command Register to 1.

After the search accelerator is activated, the host must send 16 bytes to complete a single Search ROM pass on the 1-Wire bus. These bytes are constructed as follows:

First Byte							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
r_3	x_3	r_2	x_2	r_1	x_1	r_0	x_0

Etc.

16th Byte							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
r_{63}	x_{63}	r_{62}	x_{62}	r_{61}	x_{61}	r_{60}	x_{60}

In this scheme, the index (values from 0 to 63, "n") designates the position of the bit in the ROM ID of a 1-Wire device. The character "x" marks bits that act as a filler and do not require a specific value (don't care bits). The character "r" specifies the selected bit value to write at that particular bit in case of a conflict during the execution of the ROM search.

For each bit position n (values from 0 to 63) the DS1WM generates three time slots on the 1-Wire bus. These are referenced as:

b0 for the first time slot (read data)
b1 for the second time slot (read data)
b2 for the third time slot (write data)

The DS1WM determines the type of time slot b2 (write-one or write-zero) as follows:

b2 = r_n if conflict (as chosen by the host)
= b0 if no conflict (there is no alternative)
= 1 if error (there is no response)

The 16 response bytes that the host reads from the Receive Buffer during a complete pass through a Search ROM function using the search accelerator are constructed as follows:

First Byte							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
r'_3	d_3	r'_2	d_2	r'_1	d_1	r'_0	d_0

Etc.

16th Byte							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
r'_{63}	d_{63}	r'_{62}	d_{62}	r'_{61}	d_{61}	r'_{60}	d_{60}

As before, the index (values from 0 to 63, "n") designates the position of the bit in the ROM ID of a 1-Wire device. The character "d" marks the discrepancy flag in that particular bit position. The discrepancy flag is 1 if there is a conflict or no response in that particular bit position, and 0 otherwise. The character " r' " marks the actually chosen path at that particular bit position. The chosen path is identical to b2 for the particular bit position of the ROM ID.

To perform a Search ROM sequence, one starts with all bits r_n being 0s. In case of a bus error, all subsequent response bits r'_n are 1's until the Search Accelerator is deactivated by writing the SRA bit in the Command Register to 0. Thus, if r'_{63} and d_{63} are both 1, an error has occurred during the search procedure and the last sequence must be repeated. Otherwise r'_n (n = 0...63) is the ROM ID of the device that has been found and addressed. If the host wishes to execute a memory function with this slave, first the search accelerator needs to be deactivated.

If the host wants to continue with the ROM search to identify the remaining 1-Wire slaves, it first must instruct the DS1WM to turn off the search accelerator, perform a 1-Wire reset/presence-detect cycle, and transmit the Search ROM command. Then the search accelerator must be activated again.

For the next Search ROM sequence, reuse the previous set r_n (n = 0…63) but set r_m to 1, with "m" being the index number of the highest discrepancy flag that is 1, and set all r_i to 0 with i > m.

All parts are found if the highest discrepancy occurs in the same bit position for two consecutive passes.

Application Information

FPGAs or ASICs integrate the designed DS1WM. In **Figure 14**, the design module with a microprocessor can offload the 1-Wire communication to the DS1WM.

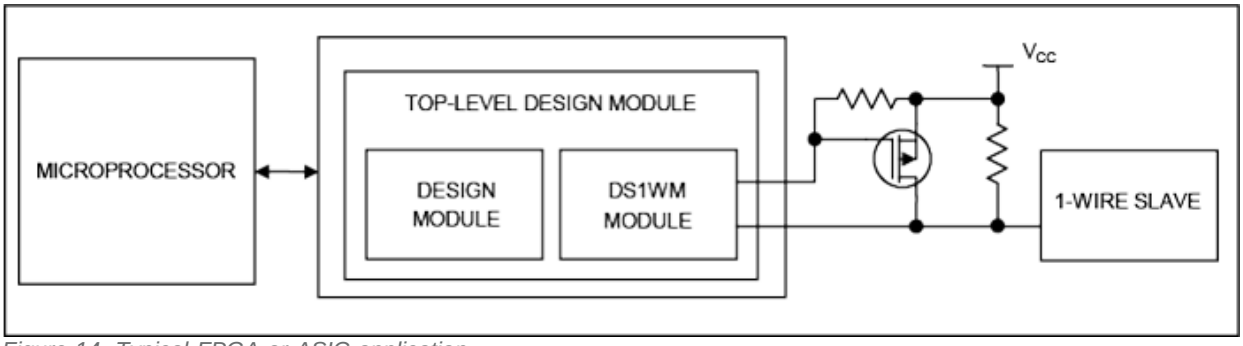

Figure 14. Typical FPGA or ASIC application.

Verification

The industry typically denotes the level of verification of an IP block with the following conventions:

- Gold IP has been to target silicon.
- Silver IP has been to target silicon in FPGA.
- Bronze IP has been verified in silicon models with logical timing closure.
- In-development IP has not yet been verified.

Note: The DS1WM has achieved silver status.

Deliverables

The DS1WM package comes complete with:

- Verilog HDL
- VHDL
- Verilog test bench
- Readme information on setup and scripts

The free DS1WM IP is available by request.

Summary

The DS1WM synthesizable 1-Wire bus master is an alternative to performing 1-Wire communication through "bit-banging." It can be embedded in an FPGA or ASIC, where it appears as a memory-mapped device. The DS1WM supports the communication- and power-delivery requirements of all 1-Wire slave devices.

Related Parts		
DS1822	Econo 1-Wire Digital Thermometer	Free Samples
DS1822-PAR	Econo Parasite-Power Digital Thermometer	
DS1825	Programmable Resolution 1-Wire Digital Thermometer With 4-Bit ID	Free Samples

DS18B20	Programmable Resolution 1-Wire Digital Thermometer	Free Samples
DS18B20-PAR	1-Wire Parasite-Power Digital Thermometer	
DS18S20	1-Wire Parasite-Power Digital Thermometer	Free Samples
DS18S20-PAR	Parasite-Power Digital Thermometer	
DS1904	iButton RTC	Free Samples
DS1920	iButton Temperature Logger	
DS1921G	Thermochron iButton Device	
DS1921H	High-Resolution Thermochron iButton Devices	
DS1921Z	High-Resolution Thermochron iButton Devices	
DS1922E	iButton High-Temperature Logger with 8KB Data-Log Memory	
DS1922L	iButton Temperature Loggers with 8KB Data-Log Memory	
DS1922T	iButton Temperature Loggers with 8KB Data-Log Memory	
DS1923	iButton Hygrochron Temperature/Humidity Logger with 8KB Data-Log Memory	
DS1961S	iButton 1Kb EEPROM with SHA-1 Engine	
DS1963S	iButton Monetary Device with SHA-1 Function	
DS1971	iButton 256-Bit EEPROM	
DS1972	iButton 1024-Bit EEPROM	
DS1973	iButton 4Kb EEPROM	Free Samples
DS1977	iButton 32KB EEPROM	Free Samples
DS1982	iButton 1Kb Add-Only	Free Samples
DS1985	iButton 16Kb Add-Only	Free Samples
DS1990A	iButton Serial Number	Free Samples
DS1990R	Serial Number ¡Button	Free Samples
DS1992	iButton 1Kb/4Kb Memory	Free Samples
DS1993	iButton 1Kb/4Kb Memory	Free Samples
DS1995	iButton 16Kb Memory	Free Samples
DS1996	iButton 64Kb Memory	Free Samples
DS2401	Silicon Serial Number	Free Samples
DS2406	Dual Addressable Switch Plus 1Kb Memory	Free Samples
DS2408	1-Wire 8-Channel Addressable Switch	Free Samples
DS2411	Silicon Serial Number with V_{CC} Input	Free Samples
DS2413	1-Wire Dual Channel Addressable Switch	Free Samples
DS2417	1-Wire Time Chip With Interrupt	Free Samples
DS2430A	256-Bit 1-Wire EEPROM	

DS2431	1024-Bit 1-Wire EEPROM	Free Samples
DS2431-A1	1024-Bit, 1-Wire EEPROM for Automotive Applications	Free Samples
DS2432	1Kb Protected 1-Wire EEPROM with SHA-1 Engine	Free Samples
DS2438	Smart Battery Monitor	Free Samples
DS24B33	1-Wire 4Kb EEPROM	Free Samples
DS2502	1Kb Add-Only Memory	Free Samples
DS2502-E48	48-Bit Node Address Chip	Free Samples
DS2502-E64	IEEE EUI-64 Node Address Chip	Free Samples
DS2505	16Kb Add-Only Memory	Free Samples
DS25LV02	Low Voltage 1024-Bit EPROM	
DS2740	High-Precision Coulomb Counter	Free Samples
DS2756	High-Accuracy Battery Fuel Gauge with Programmable Suspend Mode	Free Samples
DS2762	High-Precision Li+ Battery Monitor with Alerts	Free Samples
DS2775	2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication	
DS2776	2-Cell, Stand-Alone, Li+ Fuel-Gauge IC with Protector and Optional SHA-1 Authentication	
DS2780	Stand-Alone Fuel Gauge IC	Free Samples
DS2781	1-Cell or 2-Cell Stand-Alone Fuel Gauge IC	Free Samples
DS2784	1-Cell Stand-Alone Fuel Gauge IC with Li+ Protector and SHA-1 Authentication	Free Samples
DS2788	Stand-Alone Fuel-Gauge IC with LED Display Drivers	Free Samples
DS28E01-100	1Kb Protected 1-Wire EEPROM with SHA-1 Engine	Free Samples
DS28E02	1-Wire SHA-1 Authenticated 1Kb EEPROM with 1.8V Operation	Free Samples
DS28E04-100	4096-Bit Addressable 1-Wire EEPROM with PIO	
DS28E10	1-Wire SHA-1 Authenticator	Free Samples
DS28E15	DeepCover Secure Authenticator with 1-Wire SHA-256 and 512-Bit User EEPROM	Free Samples
DS28E22	DeepCover Secure Authenticator with 1-Wire SHA-256 and 2Kb User EEPROM	Free Samples
DS28E25	DeepCover Secure Authenticator with 1-Wire SHA-256 and 4Kb User EEPROM	Free Samples
DS28EA00	1-Wire Digital Thermometer with Sequence Detect and PIO	Free Samples
DS28EC20	20Kb 1-Wire EEPROM	Free Samples
DS9105	iButton Number Set	
DS9108	Concrete Temperature Monitor	
MAX31820	1-Wire Ambient Temperature Sensor	Free Samples

MAX31820PAR	1-Wire Parasite-Power, Ambient Temperature Sensor	
MAX31826	1-Wire Digital Temperature Sensor with 1Kb Lockable EEPROM	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 5507: http://www.maximintegrated.com/an5507
APPLICATION NOTE 5507, AN5507, AN 5507, APP5507, Appnote5507, Appnote 5507