

# ON Semiconductor

## Is Now

# onsemi™

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.



ON Semiconductor®

# FDG8842CZ

## Complementary PowerTrench® MOSFET

Q1: 30V, 0.75A, 0.4Ω; Q2: -25V, -0.41A, 1.1Ω

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 0.4Ω at  $V_{GS} = 4.5V$ ,  $I_D = 0.75A$
- Max  $r_{DS(on)}$  = 0.5Ω at  $V_{GS} = 2.7V$ ,  $I_D = 0.67A$

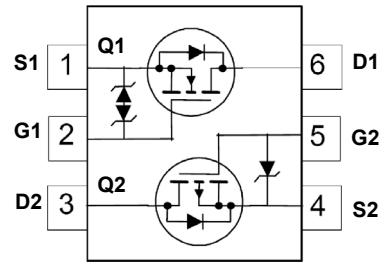
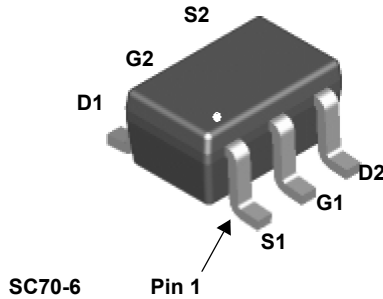
Q2: P-Channel

- Max  $r_{DS(on)}$  = 1.1Ω at  $V_{GS} = -4.5V$ ,  $I_D = -0.41A$
- Max  $r_{DS(on)}$  = 1.5Ω at  $V_{GS} = -2.7V$ ,  $I_D = -0.25A$
- Very low level gate drive requirements allowing direct operation in 3V circuits ( $V_{GS(th)} < 1.5V$ )
- Very small package outline SC70-6
- RoHS Compliant



### General Description

These N & P-Channel logic level enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	-25	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	-8	V
$I_D$	Drain Current -Continuous	0.75	-0.41	A
	-Pulsed	2.2	-1.2	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.36		W
		0.30		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ C$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single operation (Note 1a)	350	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Single operation (Note 1b)	415	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.42	FDG8842CZ	7"	8mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	Q1 Q2	30 -25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		25 -21		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$ $V_{GS} = -8\text{V}, V_{DS} = 0\text{V}$	Q1 Q2			$\pm 10$ -100	$\mu\text{A}$ nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	Q1 Q2	0.65 -0.65	1.0 -0.8	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		-3.0 1.8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 0.75\text{A}$ $V_{GS} = 2.7\text{V}, I_D = 0.67\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 0.75\text{A}, T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{V}, I_D = -0.41\text{A}$ $V_{GS} = -2.7\text{V}, I_D = -0.25\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -0.41\text{A}, T_J = 125^\circ\text{C}$	Q1 Q2		0.25 0.29 0.36 0.87 1.20 1.22	0.4 0.5 0.6 1.1 1.5 1.9	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 0.75\text{A}$ $V_{DS} = -5\text{V}, I_D = -0.41\text{A}$	Q1 Q2		3 8		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		90 70	120 100	pF
$C_{oss}$	Output Capacitance	Q2 $V_{DS} = -10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		20 30	30 40	pF
$C_{rss}$	Reverse Transfer Capacitance		Q1 Q2		15 15	25 25	pF

**Switching Characteristics (note 2)**

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 5\text{V}, I_D = 0.5\text{A}$	Q1 Q2		4 6	10 12	ns
$t_r$	Rise Time	$V_{GS} = 4.5\text{V}, R_{GEN} = 6\Omega$ Q2	Q1 Q2		1 16	10 29	ns
$t_{d(off)}$	Turn-Off Delay Time	$V_{DD} = -5\text{V}, I_D = -0.5\text{A}$ $V_{GS} = -4.5\text{V}, R_{GEN} = 6\Omega$	Q1 Q2		9 35	18 56	ns
$t_f$	Fall Time		Q1 Q2		1 40	10 64	ns
$Q_g$	Total Gate Charge	Q1	Q1 Q2		1.03 1.20	1.44 1.68	nC
$Q_{gs}$	Gate to Source Charge	$V_{GS} = 4.5\text{V}, V_{DD} = 5\text{V}, I_D = 0.75\text{A}$ Q2	Q1 Q2		0.29 0.31		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$V_{GS} = -4.5\text{V}, V_{DD} = -5\text{V}, I_D = -0.41\text{A}$	Q1 Q2		0.17 0.22		nC

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			0.3 -0.3	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 0.3A$ (Note 2) $V_{GS} = 0V, I_S = -0.3A$ (Note 2)	Q1 Q2		0.76 -0.84	1.2 -1.2	V

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



Scale 1:1 on letter size paper.



b. 415°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

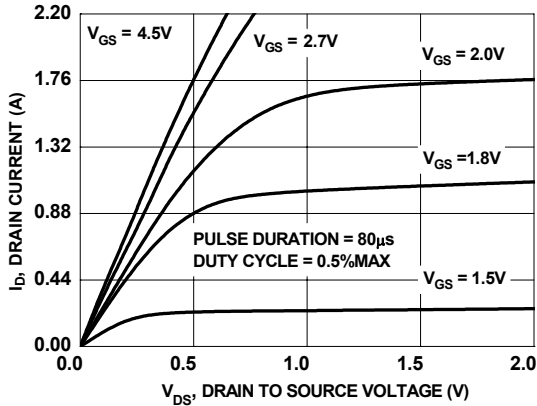


Figure 1. On-Region Characteristics

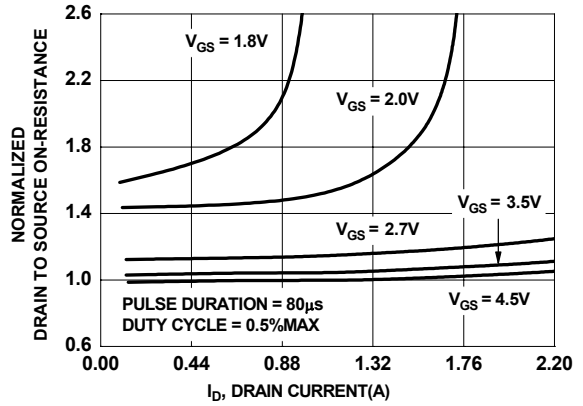


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

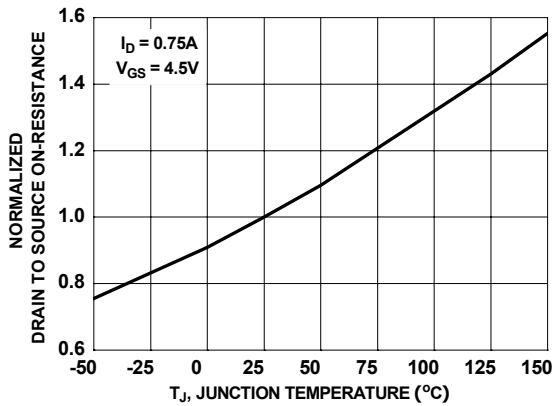


Figure 3. Normalized On-Resistance vs Junction Temperature

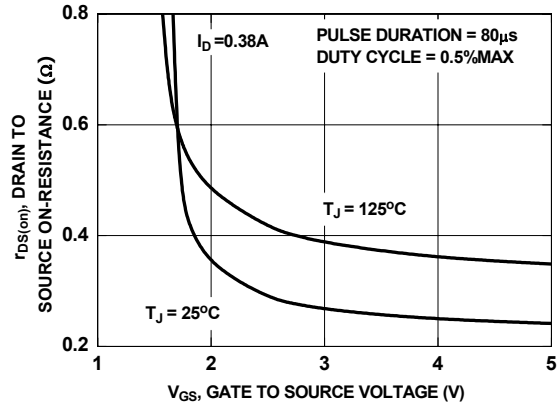


Figure 4. On-Resistance vs Gate to Source Voltage

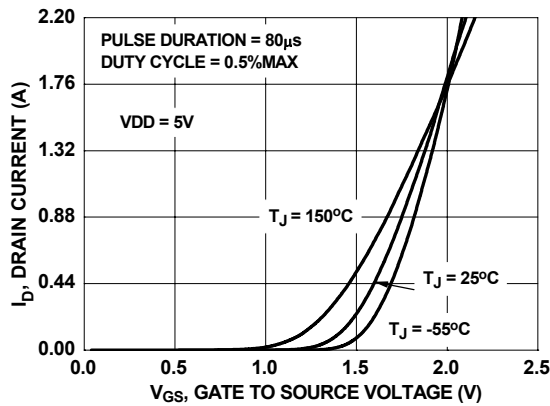


Figure 5. Transfer Characteristics

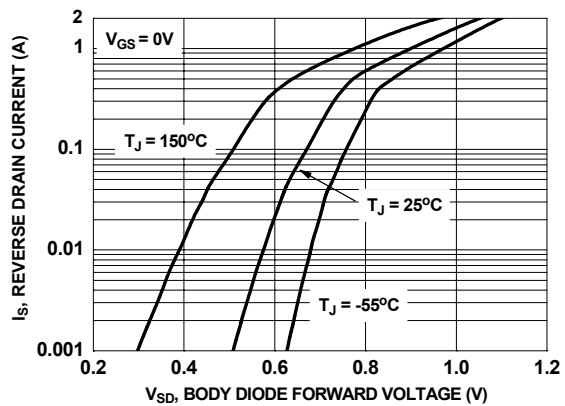
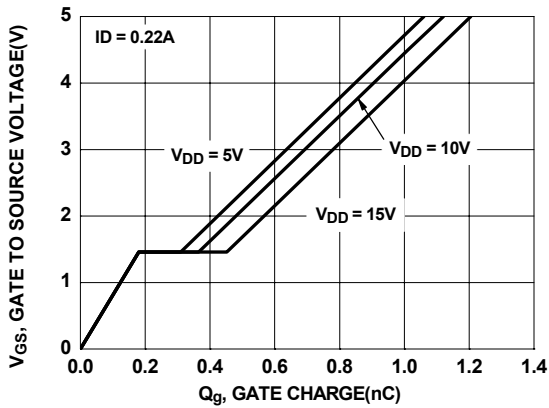
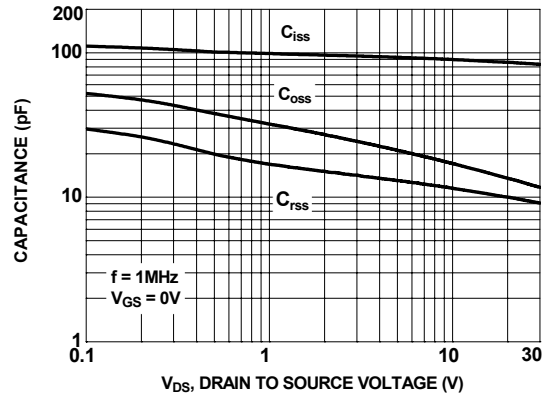


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

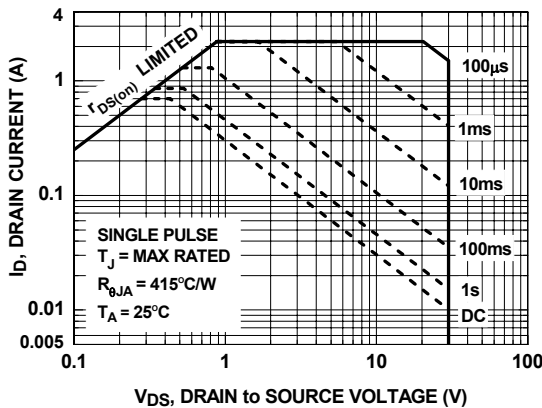
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



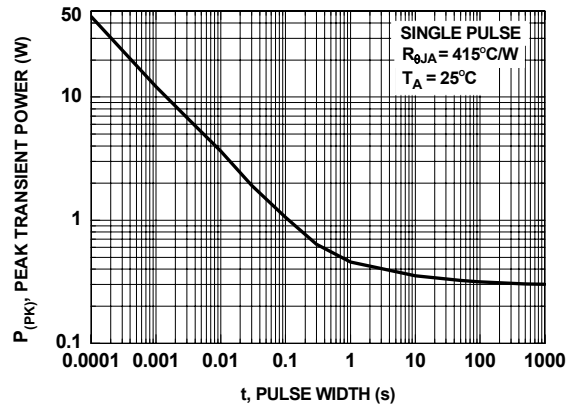
**Figure 7. Gate Charge Characteristics**



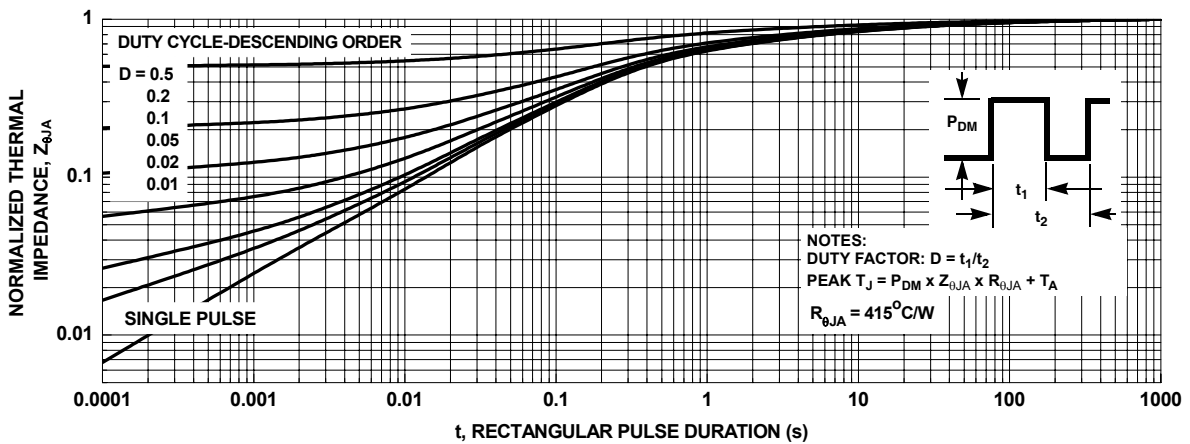
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**



**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Transient Thermal Response Curve**

**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

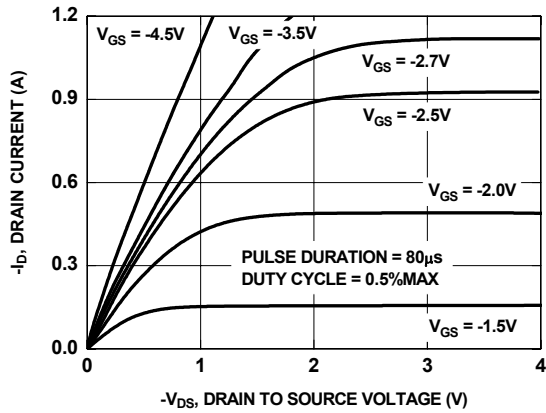


Figure 13. On Region Characteristics

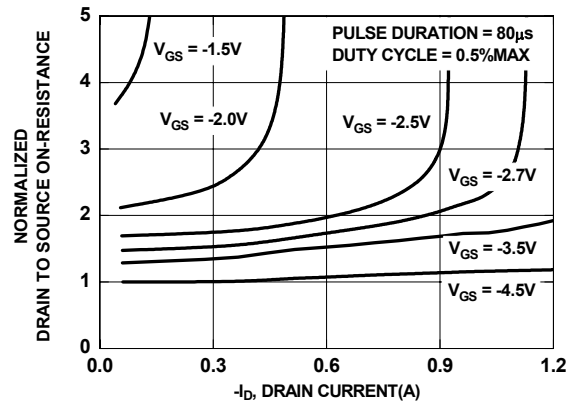


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

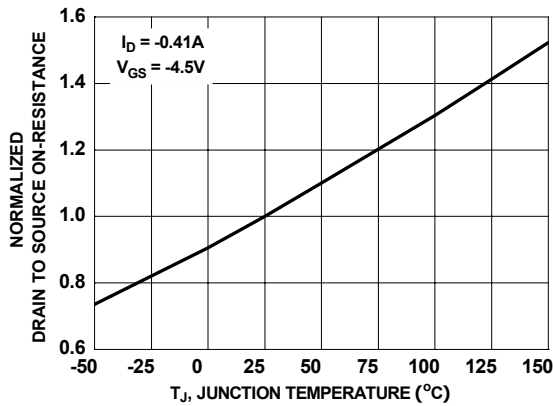


Figure 15. Normalized On Resistance vs Junction Temperature

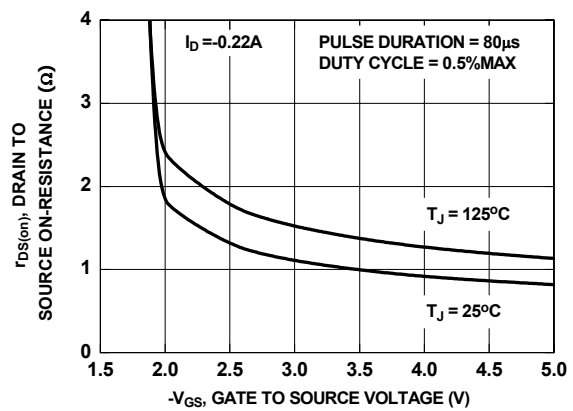


Figure 16. On-Resistance vs Gate to Source Voltage

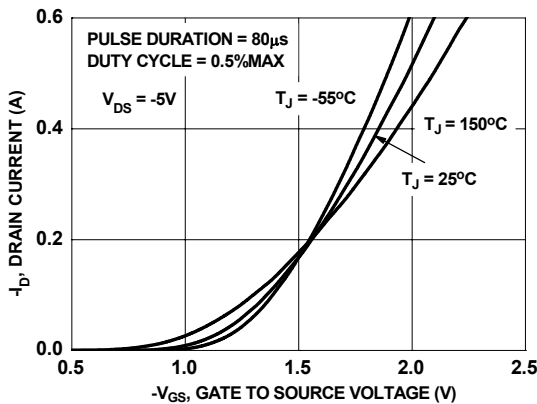


Figure 17. Transfer Characteristics

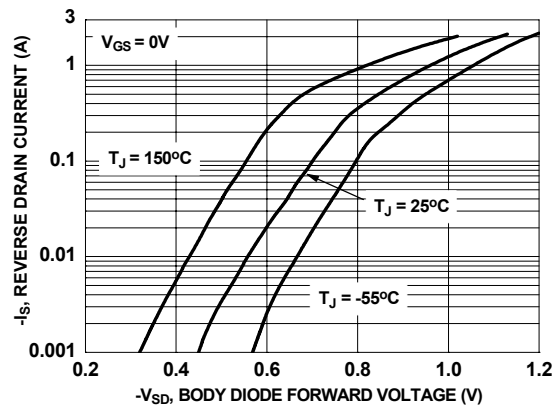
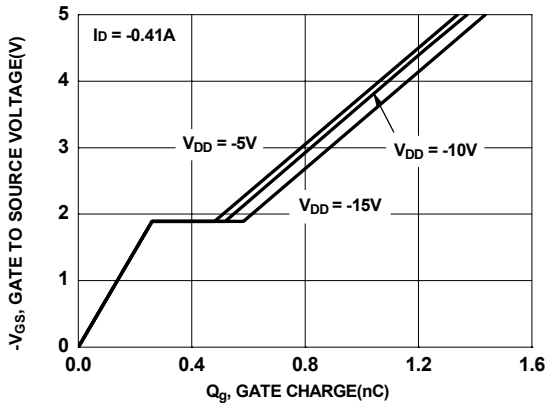
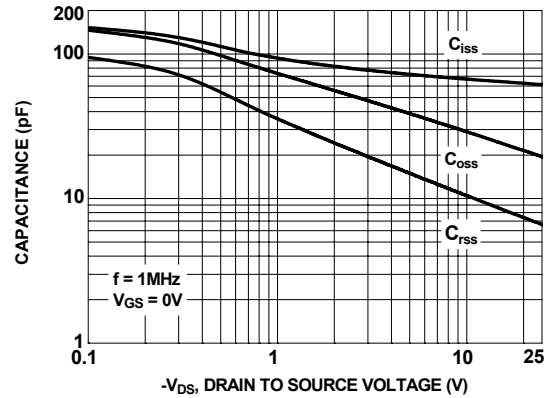


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

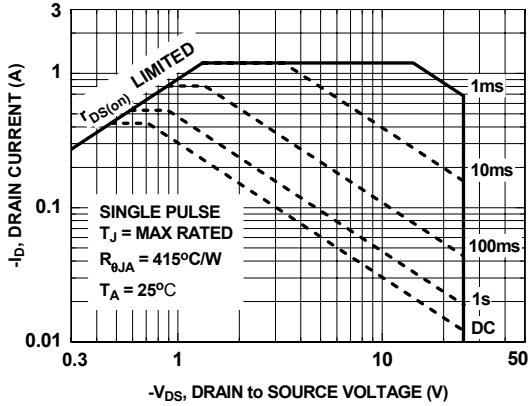
**Typical Characteristics(Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



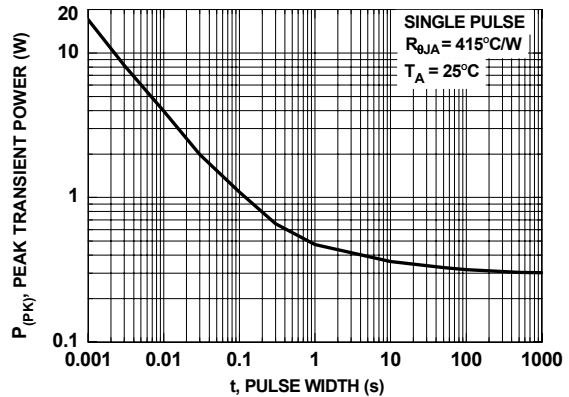
**Figure 19. Gate Charge Characteristics**



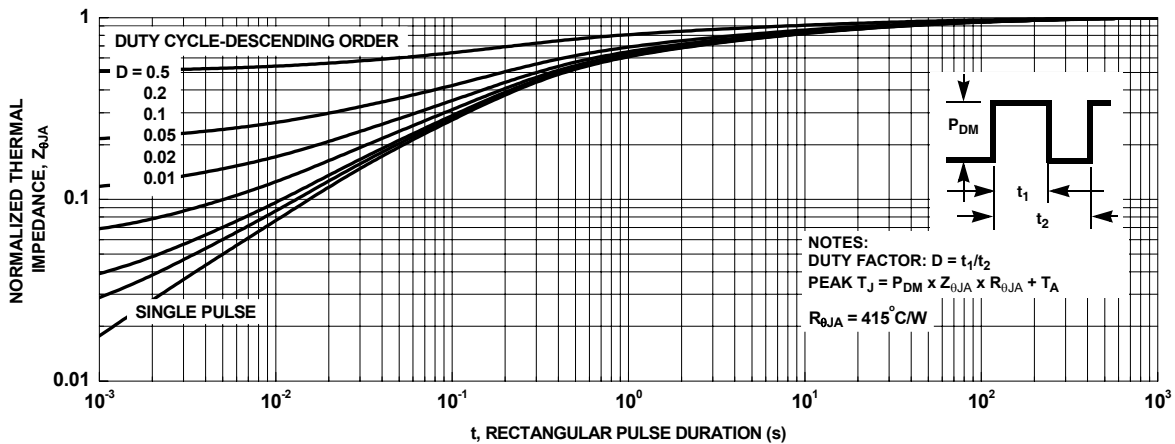
**Figure 20. Capacitance vs Drain to Source Voltage**



**Figure 21. Forward Bias Safe Operating Area**



**Figure 22. Single Pulse Maximum Power Dissipation**



**Figure 23. Transient Thermal Response Curve**



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative