

Keywords: T1, E1, template, pulse, pulse control, wave shape, waveform, transmit, LIU, line interface unit

#### APPLICATION NOTE 4325

# Transmit Pulse Control on the DS26518 T1/E1/J1 Transceiver

Dec 12, 2008

*Abstract: As network-protection components are added to a system and/or signals must be routed through connectors and other PC-board requirements, sometimes it is necessary to manipulate the transmit waveform. This application note explains how the DS26518 T1/E1/J1 transceiver contains precise methods for making minor or major changes to the output pulse. The note also describes how to access factory test registers that allow a designer to modify the transmit waveform to meet a wide variety of application requirements.*

## T1 and E1 Transmit Waveform: Programmable Sections

The [DS26518](#) registers provide control for the transmit pulse in two major areas: amplitude and timing. T1 and E1 transmit pulses are divided into sections, each of which can be manipulated to provide the desired waveform. **Figure 1** shows how the T1 pulse is divided and the registers that control each section. **Figure 2** provides the same information for the E1 pulse.

## T1 and E1 Transmit Waveform: Amplitude Control

The amplitude of the DS26518 transmit pulse can be controlled in two ways:

- **Adjusting the DAC Gain**  
The L1TXLAE register bits DAC[3:0] provide positive and negative adjustment of all the T1 or E1 levels simultaneously.
- **Partial Waveform Level Adjustment**  
The WLA[3:0] bits of the Level Adjustment registers provide fine-tuning of specific sections of the waveform. The step size of the voltage level will change in proportion to the programmed DAC gain. If the DAC gain is increased by 10%, then the step sizes will also increase by 10%.

## T1 and E1 Transmit Waveform: Timing Control

The timing of the DS26518 transmit pulse levels is controlled by the CEA[2:0] bits of the Level Adjustment registers. Each edge can be moved in both positive and negative directions in increments of 1/32 of TCLK.

## General Recommendations

Modifying the DAC gain is the easiest way to control the amplitude of the transmit pulse, because the

DAC gain will control the entire waveform with only one register change. Using the DAC gain first will allow for minimal, if any, modifications of the individual Level Adjustment registers. The maximum output of the DAC will be affected by  $V_{DD}$ . At lower levels of  $V_{DD}$ , the maximum DAC gain setting may be unattainable. Changing  $V_{DD}$  will also affect the maximum voltage attainable by the line driver's output stage.

Negative values do not use signed integer representation. The MSB is the sign bit and the LSBs represent magnitude irrespective of sign. For example, a -3 in a WLA[3:0] register would be 1011b (bit 3 set to 1 means negative, 011 in the next 3 bits is magnitude 3), not 1101b (4-bit signed integer representation).

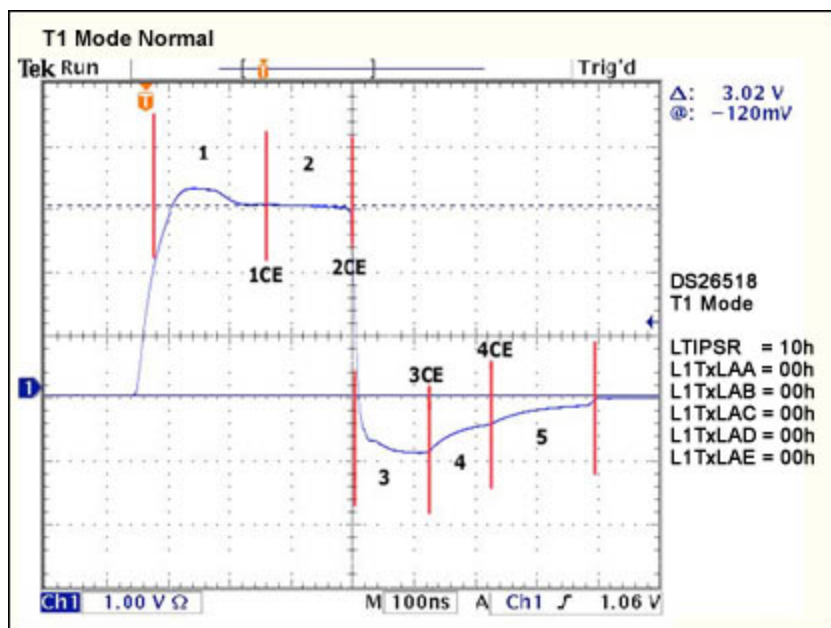


Figure 1. T1 pulse control sections.

## T1 Pulse-Control Sections

<b>Overshoot (1)</b>	Register L1TXLAA WLA[4:0]
<b>Clock Edge (1CE)</b>	Register L1TXLAA CEA[2:0]
<b>(1CE)</b> = Clock Edge transition from Overshoot to Plateau	
<b>Plateau (2)</b>	Register L1TXLAB WLA[4:0]
<b>Clock Edge (2CE)</b>	Register L1TXLAB CEA[2:0]
<b>(2CE)</b> = Clock Edge transition from Plateau to Falling Edge	
<b>Undershoot (3)</b>	Register L1TXLAC WLA[4:0]
<b>Clock Edge (3CE)</b>	Register L1TXLAC CEA[2:0]
<b>(3CE)</b> = Clock Edge transition from Falling Edge to end of Undershoot (3)	
<b>Undershoot (4)</b>	Register L1TXLAD WLA[4:0]
<b>Clock Edge (4CE)</b>	Register L1TXLAD CEA[2:0]
<b>(4CE)</b> = Clock Edge transition from end of Undershoot (3) to end of Undershoot (4)	
<b>Undershoot (5)</b>	Register L1TXLAC WLA[4:0]

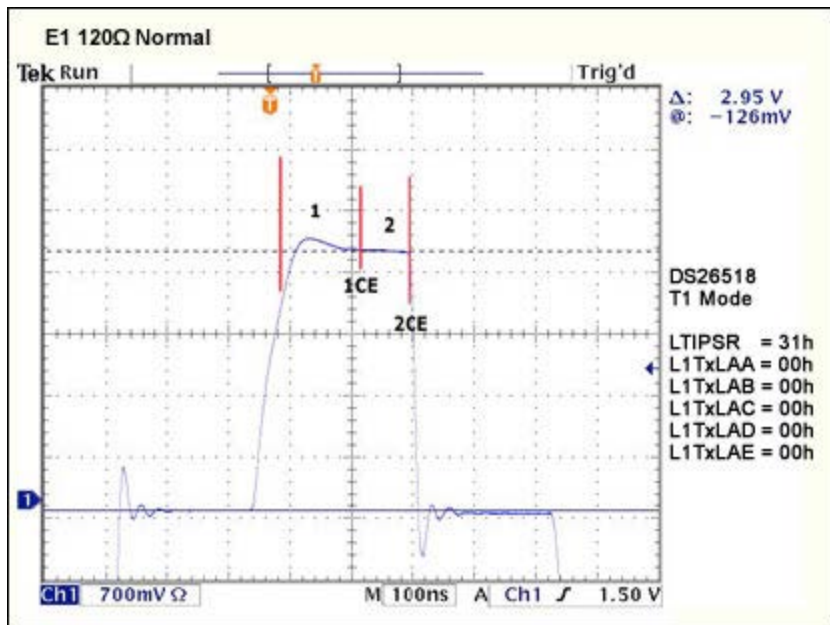


Figure 2. E1 pulse control sections.

## E1 Pulse-Control Sections

Overshoot (1)	Register L1TXLAA WLA[4:0]
Clock Edge (1CE)	Register L1TXLAA CEA[2:0]
(1CE) = Clock Edge transition from Overshoot to Plateau	
Plateau (2)	Register L1TXLAB WLA[4:0]
Clock Edge (2CE)	Register L1TXLAB CEA[2:0]
(2CE) = Clock Edge transition from Plateau to Falling Edge	

**NOTE:** Registers L1TXAC, L1TXAD, and L1TXAE are not used in E1 mode.

## LIU Test-Register Descriptions

**Table 1** provides the register address and description for LIU 1. These registers are duplicated for LIUs 2 through 8.

**Table 2** provides the addresses for all of the LIU test registers.

**Table 1. LIU 1 Test Registers**

Address	Abbr.	Description
1011h	L1TXLAA	LIU 1 Tx Level Adjust A (Test Register)
1012h	L1TXLAB	LIU 1 Tx Level Adjust B (Test Register)
1013h	L1TXLAC	LIU 1 Tx Level Adjust C (Test Register)
1014h	L1TXLAD	LIU 1 Tx Level Adjust D (Test Register)
1015h	L1TXLAE	LIU 1 Tx Level Adjust E (Test Register)

**Table 2. LIU Test-Register Address Range**

LIU	Address Range
1	1011–1015h
2	1031–1035h
3	1051–1055h
4	1071–1075h
5	1091–1095h
6	10B1–10B5h
7	10D1–10D5h
8	10F1–10F5h

## Detailed LIU Test-Register Documentation

The register address and description for LIU 1 are provided below. These registers are duplicated for LIUs 2 through 8.

<b>Register Name</b>	L1TXLAA
<b>Register Description</b>	LIU Tx Level Adjust A (Overshoot Voltage)
<b>Register Address</b>	1011H
<b>Read/Write Function</b>	R/W

Bit #	7	6	5	4	3	2	1	0
<b>Name</b>	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
<b>Default</b>	0	0	0	0	0	0	0	0

### Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 1 (WLA[4:0])

Moves magnitude from default  $\pm 360\text{mV}$ .

Bit 7 = sign bit ("1" means negative)

Bits 6 to 3 = magnitude (unsigned), i.e., 20mV is LSB step size

### Bits 2 to 0: Clock Edge Adjust (CEA[2:0])

Moves clock edge  $\pm 3 \cdot 32\text{x-clks}$  from default.

<2> = sign bit ("1" means negative)

<1:0> = number of 32x-clks to move (unsigned)

<b>Register Name</b>	L1TXLAB
<b>Register Description</b>	LIU Tx Level Adjust B (Plateau Voltage)
<b>Register Address</b>	1012H
<b>Read/Write Function</b>	R/W

Bit #	7	6	5	4	3	2	1	0
<b>Name</b>	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0

Default	0	0	0	0	0	0	0	0
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**Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 2 (WLA[4:0])**

Moves magnitude from default  $\pm 360\text{mV}$ .

Bit 7 = sign bit ("1" means negative)

Bits 6 to 3 = magnitude (unsigned), i.e., 20mV is LSB step size

**Bits 2 to 0: Clock Edge Adjust (CEA[2:0])**

Moves clock edge  $\pm 3 \cdot 32\text{x-clks}$  from default.

<2> = sign bit ("1" means negative)

<1:0> = number of 32x-clks to move (unsigned)

<b>Register Name</b>	L1TXLAC							
<b>Register Description</b>	LIU Tx Level Adjust C (Undershoot Voltage)							
<b>Register Address</b>	1013H							
<b>Read/Write Function</b>	R/W							

<b>Bit #</b>	7	6	5	4	3	2	1	0
<b>Name</b>	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 3 (WLA[4:0])**

Moves magnitude from default  $\pm 360\text{mV}$ .

Bit 7 = sign bit ("1" means negative)

Bits 6 to 3 = magnitude (unsigned), i.e., 20mV is LSB step size

**Bits 2 to 0: Clock Edge Adjust (CEA[2:0])**

Moves clock edge  $\pm 3 \cdot 32\text{x-clks}$  from default.

<2> = sign bit ("1" means negative)

<1:0> = number of 32x-clks to move (unsigned)

<b>Register Name</b>	L1TXLAD							
<b>Register Description</b>	LIU Tx Level Adjust D (Undershoot Voltage #2)							
<b>Register Address</b>	1014H							
<b>Read/Write Function</b>	R/W							

<b>Bit #</b>	7	6	5	4	3	2	1	0
<b>Name</b>	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 7 to 3: Transmit Waveform Levels Adjust for Output Level 4 (WLA[4:0])**

Moves magnitude from default  $\pm 360\text{mV}$ .

Bit 7 = sign bit ("1" means negative)  
 Bits 6 to 3 = magnitude (unsigned), i.e., 20mV is LSB step size

**Bits 2 to 0: Clock Edge Adjust (CEA[2:0])**

Moves clock edge  $\pm 3$  32x-clks from default.

<2> = sign bit ("1" means negative)  
 <1:0> = number of 32x-clks to move (unsigned)

<b>Register Name</b>	L1TXLAE
<b>Register Description</b>	LIU Tx Level Adjust E (Undershoot Voltage #3)
<b>Register Address</b>	1015H
<b>Read/Write Function</b>	R/W

<b>Bit #</b>	7	6	5	4	3	2	1	0
<b>Name</b>	WLA4	WLA3	WLA2	WLA1	WLA0	CEA2	CEA1	CEA0
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 7 to 4: Transmit Waveform Levels Adjust for Output Level 5 (WLA[3:0])**

Moves magnitude from default  $\pm 180$ mV.

Bit 7 = sign bit ("1" means negative)  
 Bits 6 to 4 = magnitude (unsigned), i.e., 20mV is LSB step size

**Bits 3 to 0: DAC Gain Adjust (DAC[3:0])**

The following settings change the gain of the DAC.

DAC[3:0]	DAC Gain Value
0000	Nominal (default)
0001	+2.67%
0010	+5.34%
0011	+8.67%
0100	+11.34%
0101	+14.0%
0110	+17.34%
0111	+20.97%
1000	-2.1%
1001	-4.0%
1010	-6.0%
1011	-8.0%
1100	-10.0%
1101	-12.0%
1110	-14.0%
1111	-15.34%

## T1 and E1 Transmit Waveform Data

The following data is representative of the expected results for the DS26518. The data is a guideline for determining the range and method of using the Level Adjustment registers to control the amplitude and timing of the T1 and E1 transmit pulses. The data was taken at room temperature with 3.3V  $V_{DD}$ .

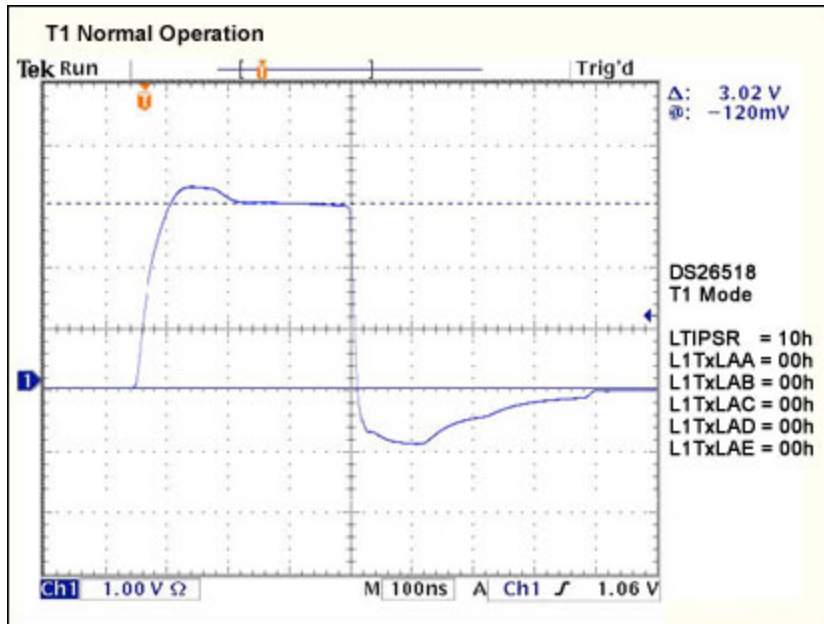


Figure 3.

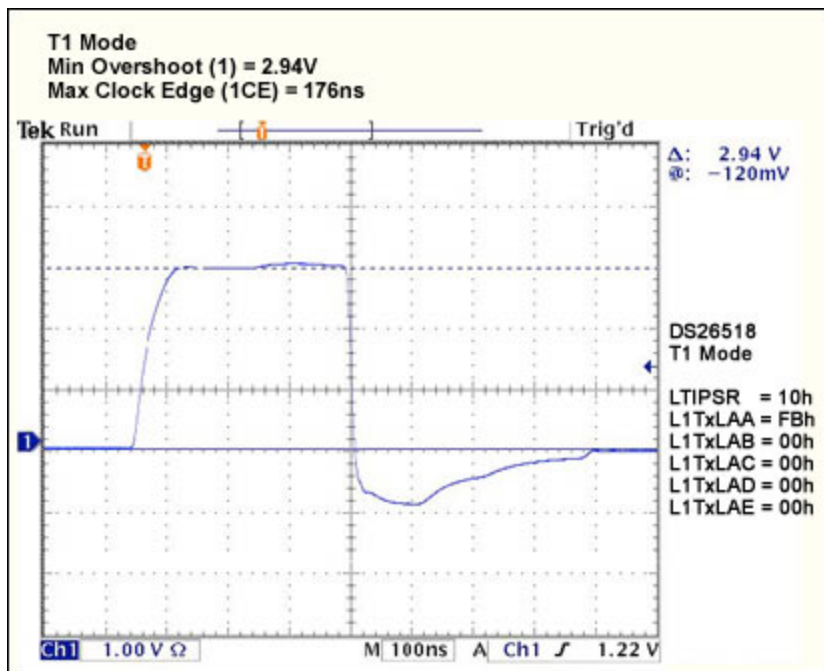


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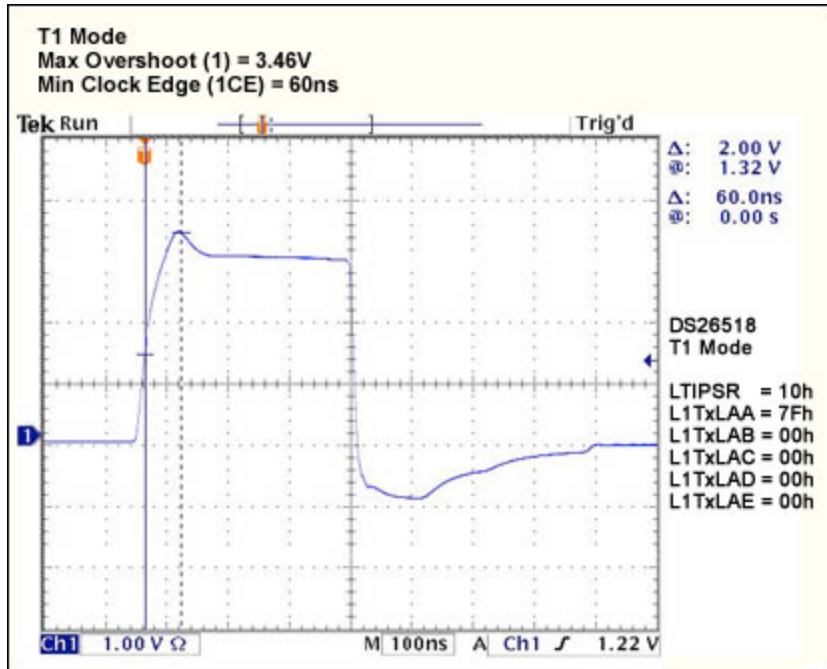


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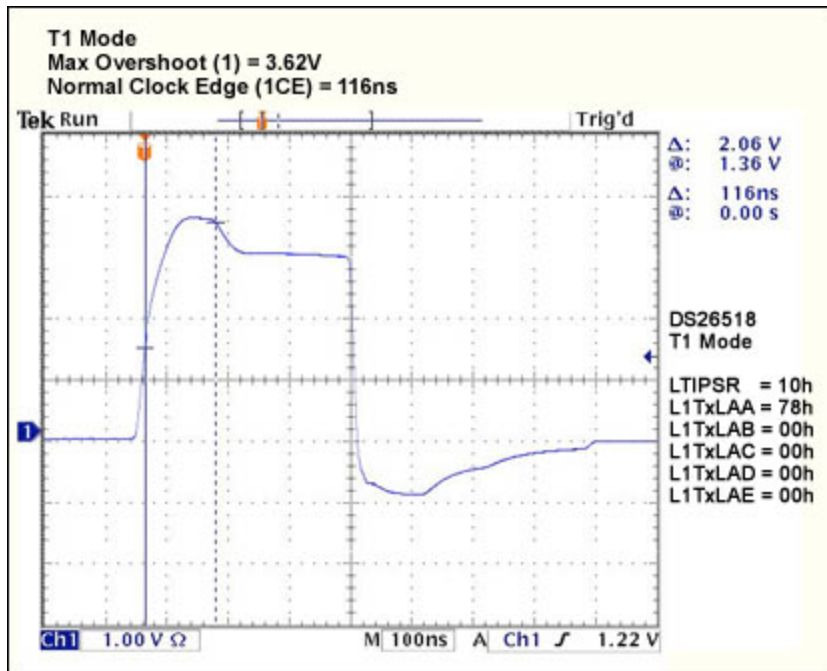


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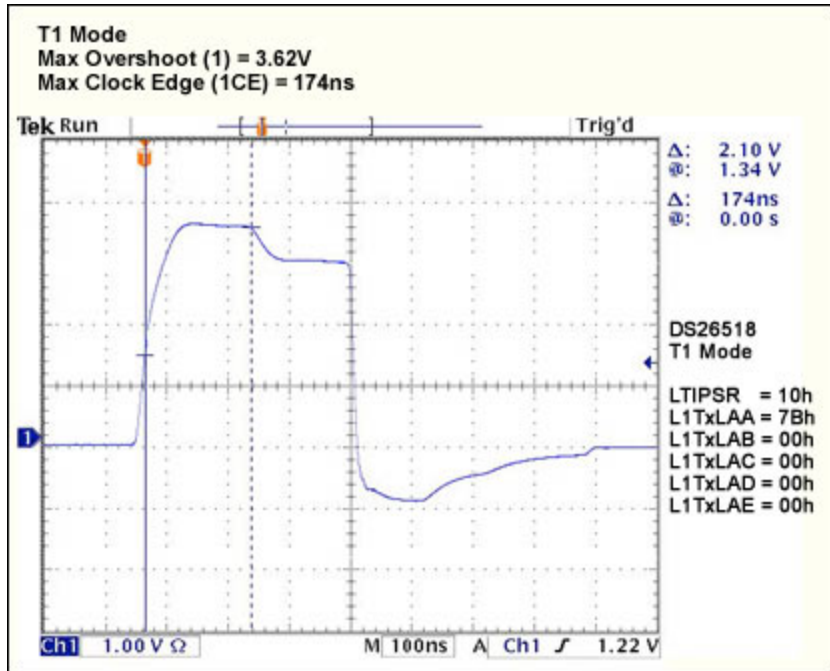


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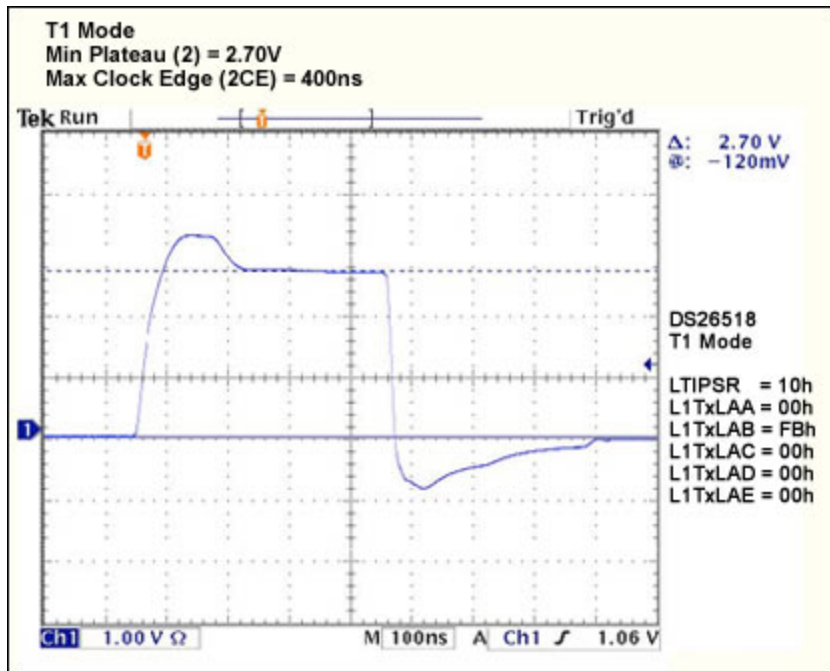


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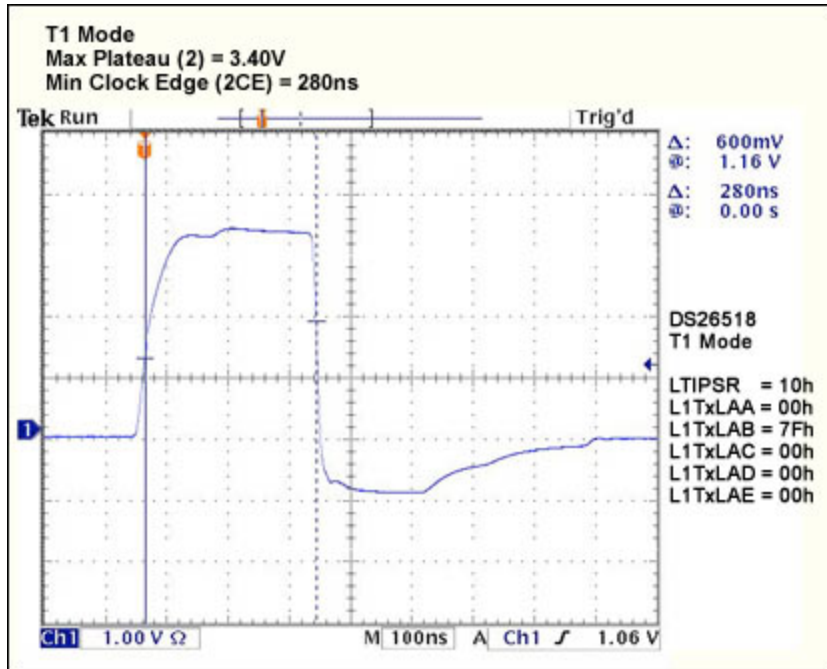


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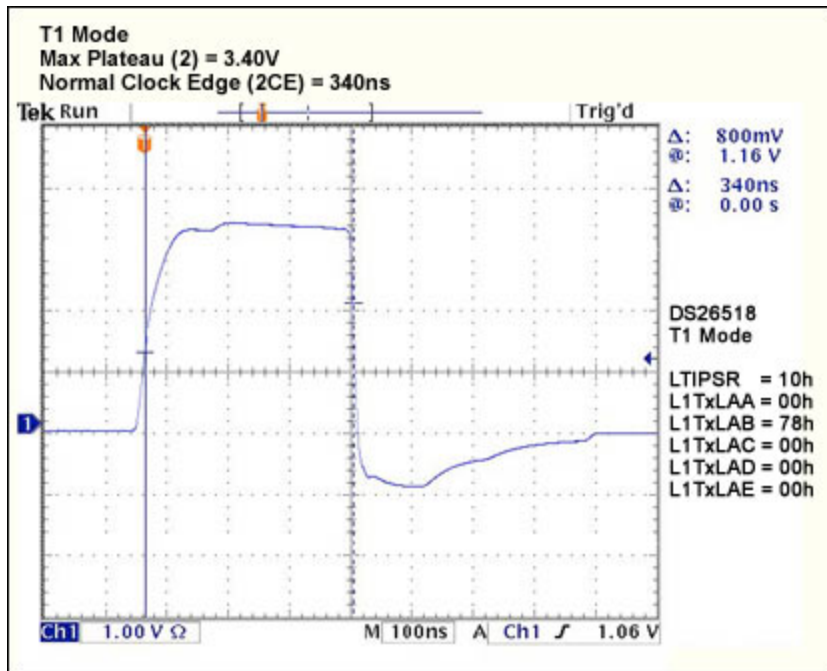


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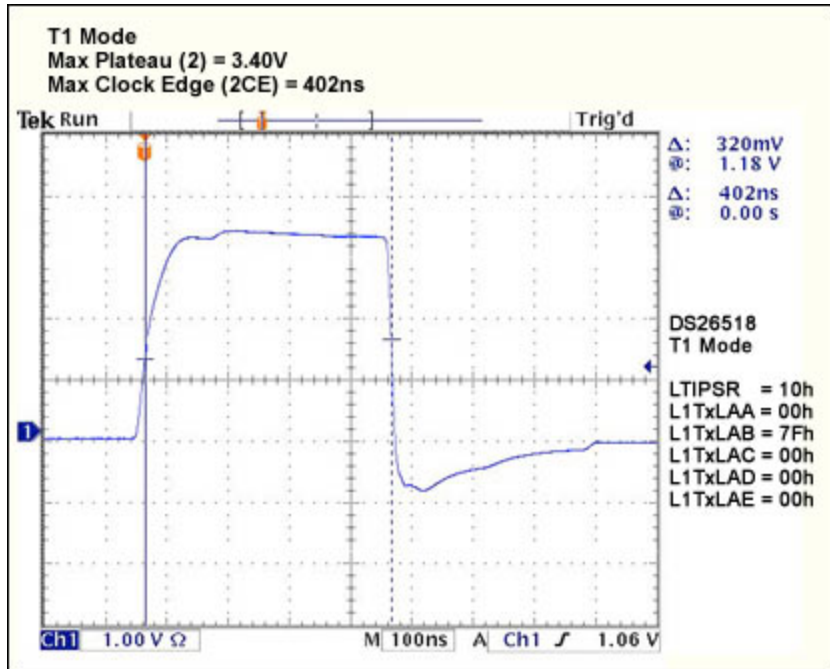


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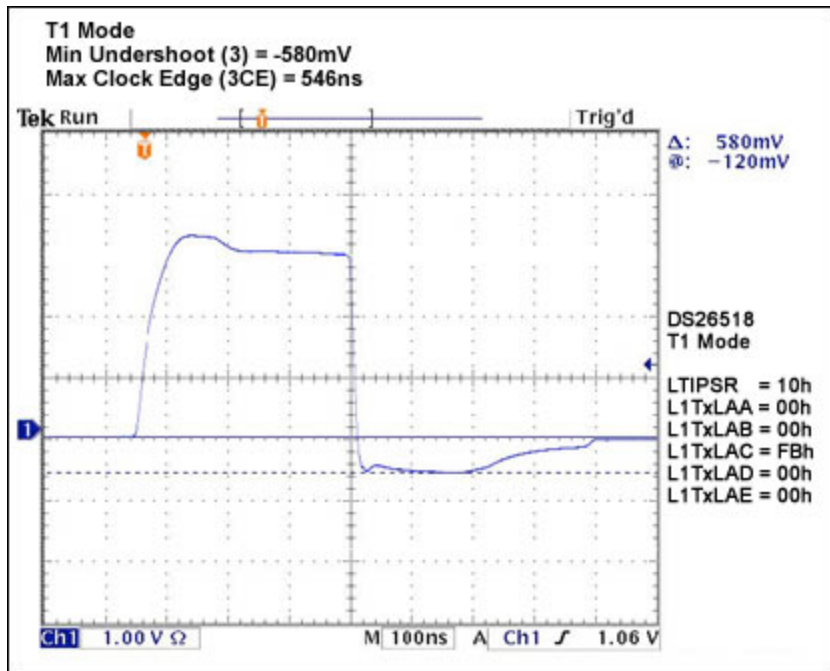


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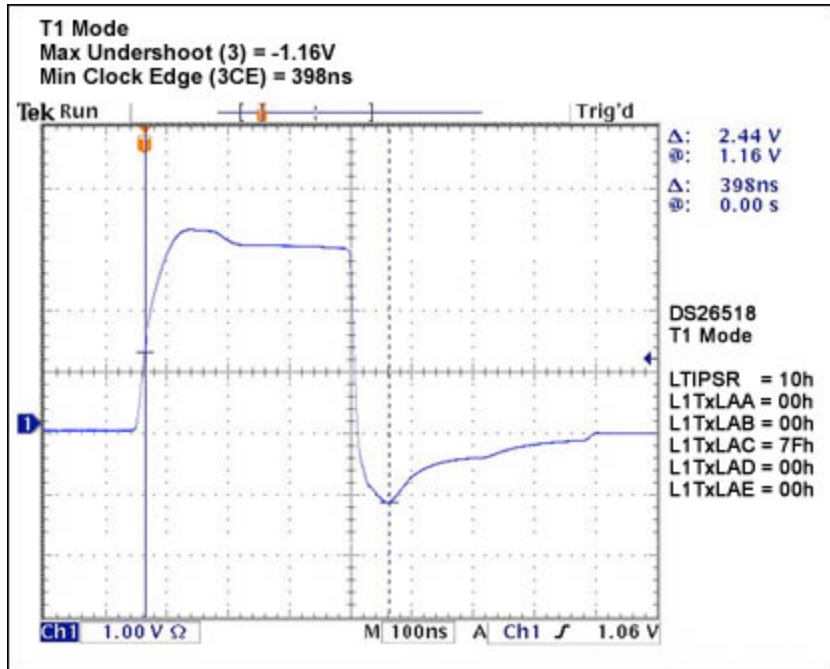


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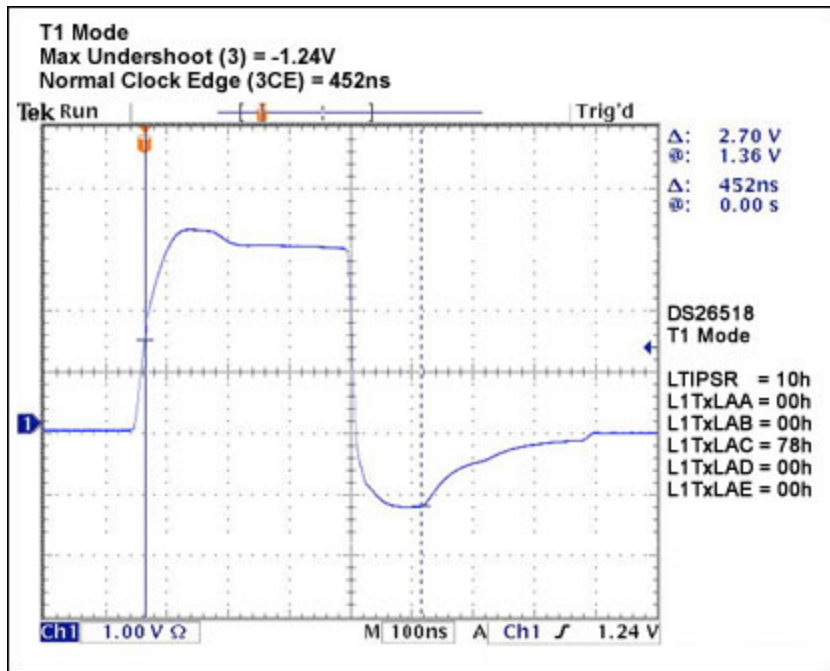


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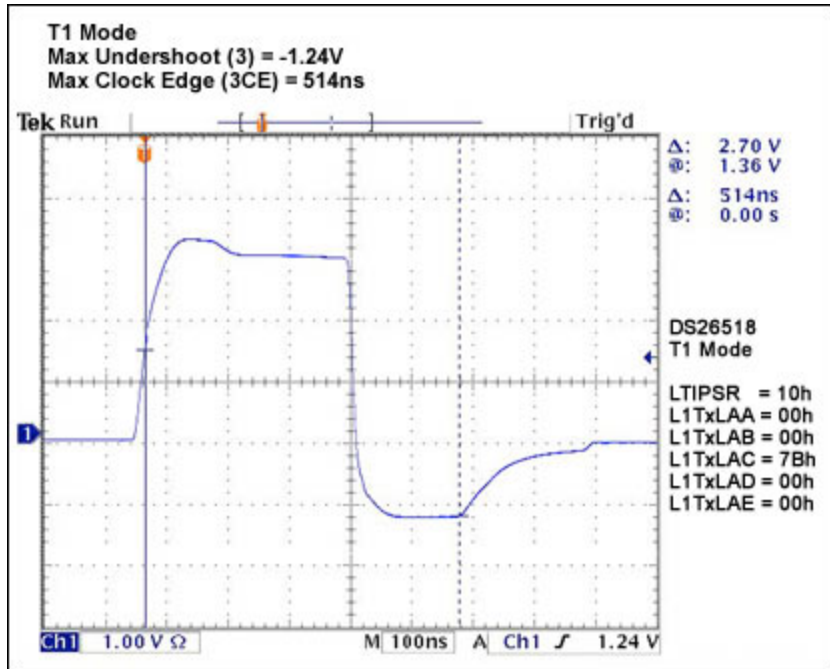


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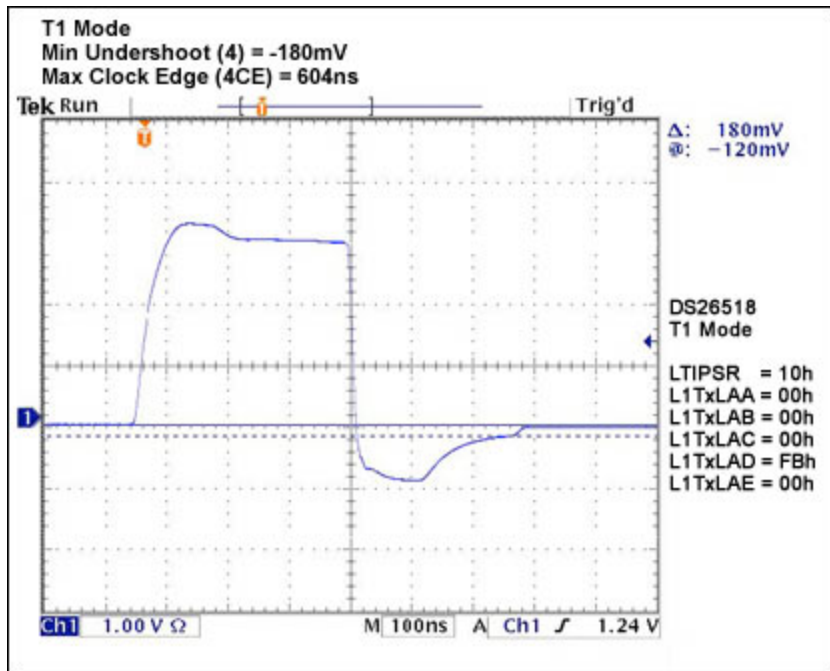


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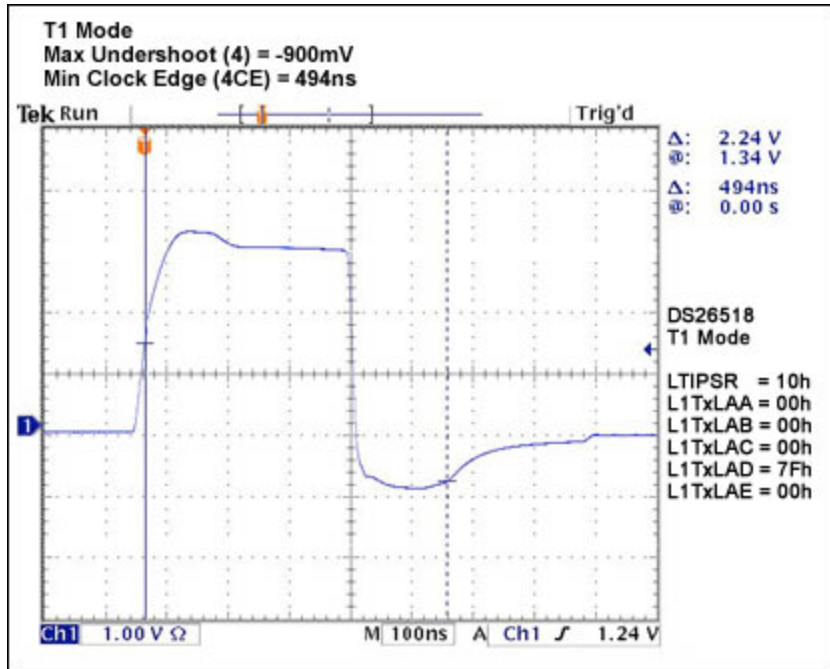


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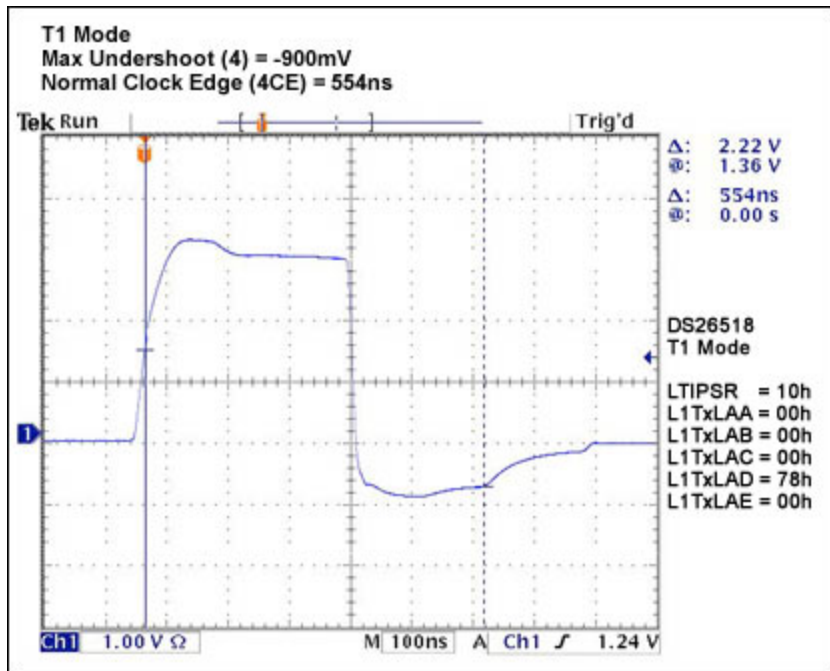


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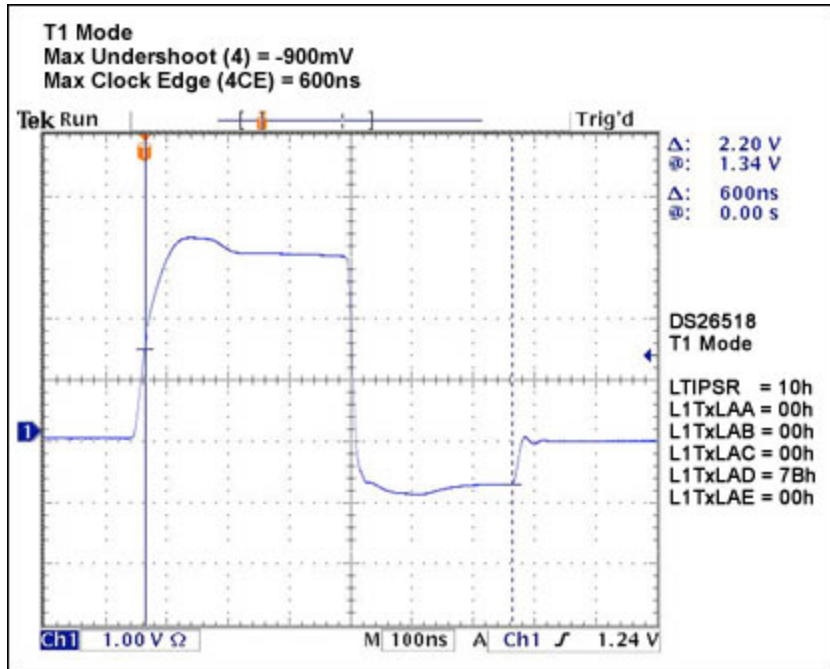


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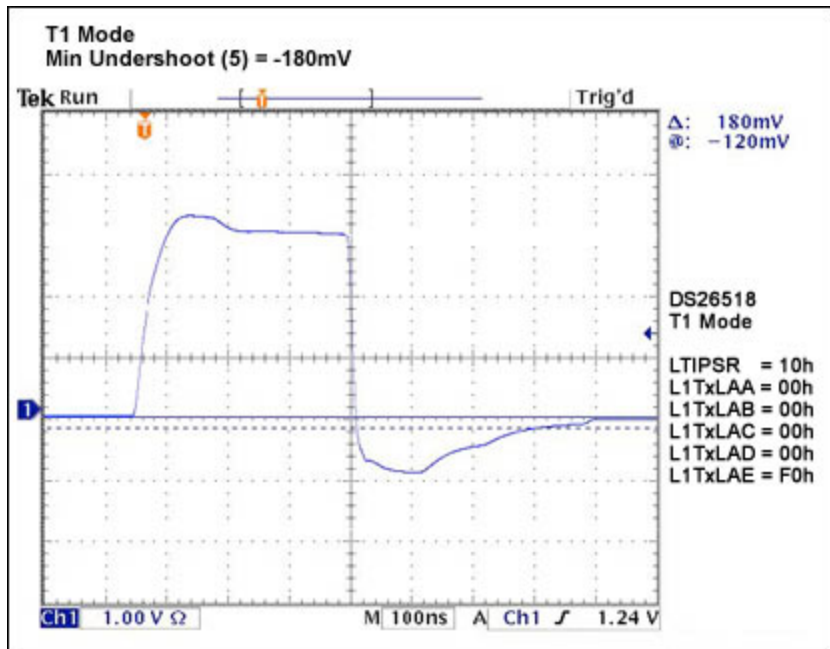


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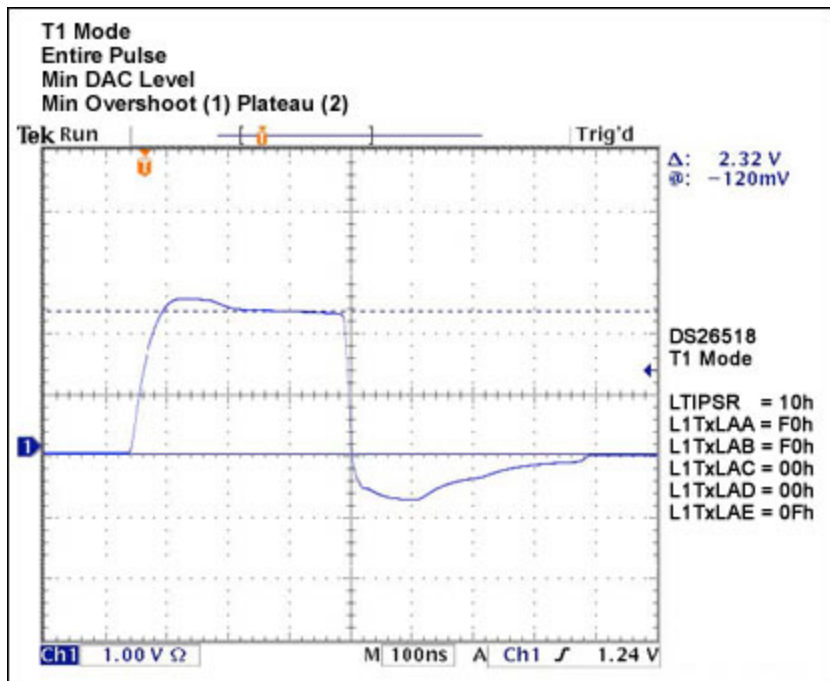


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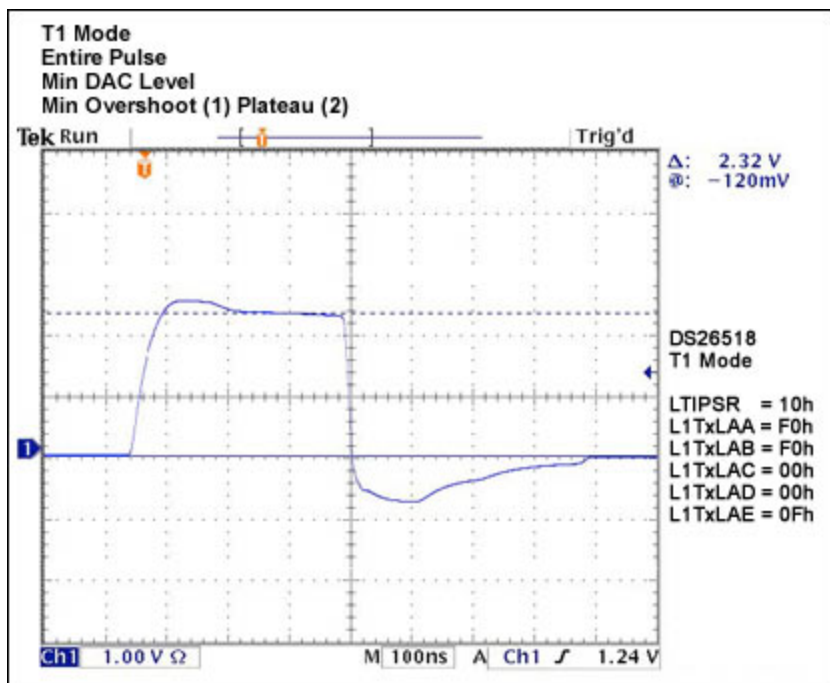


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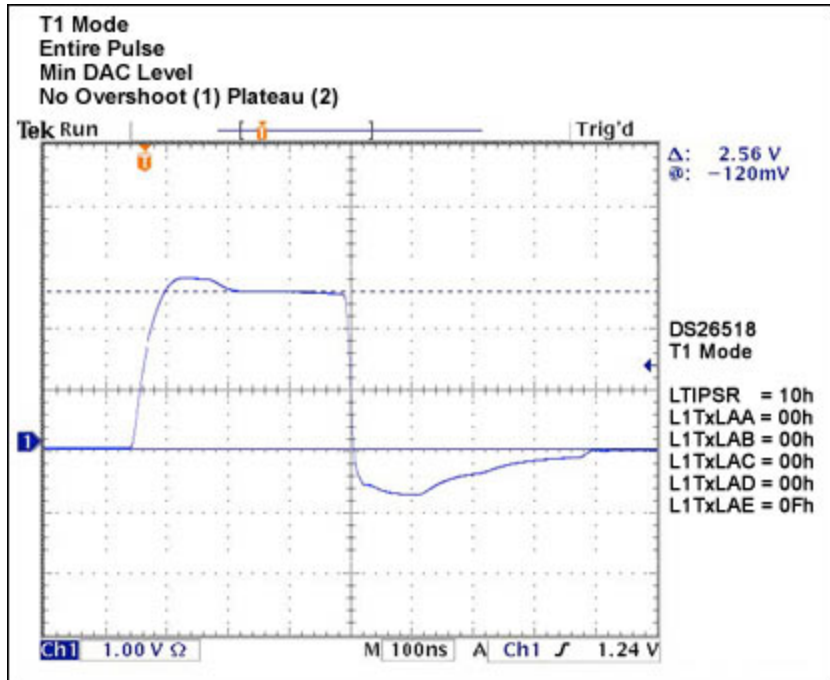


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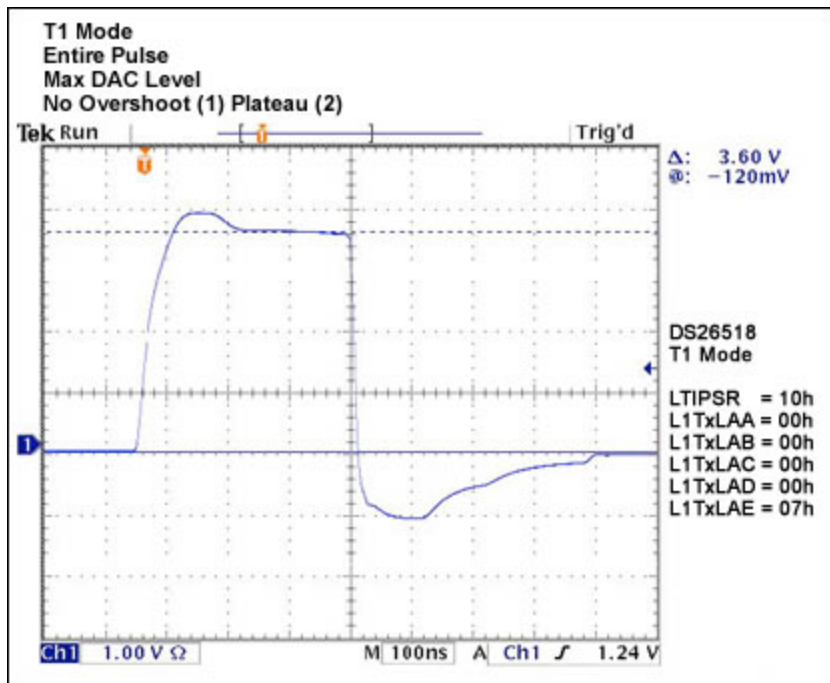


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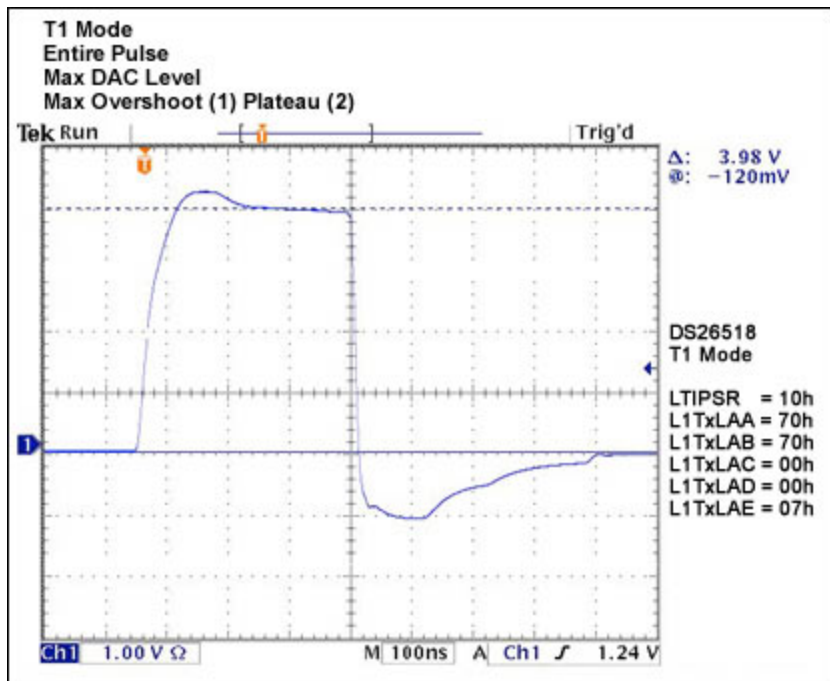


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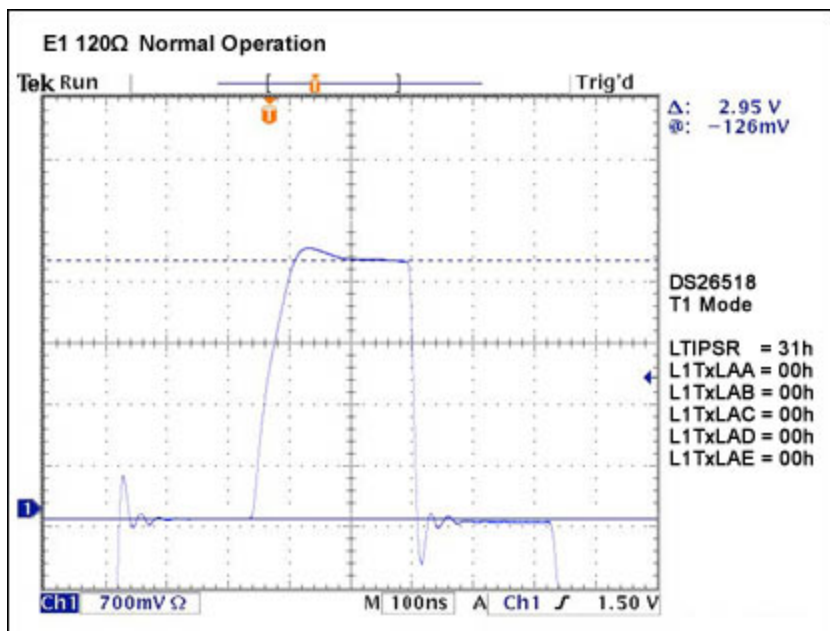


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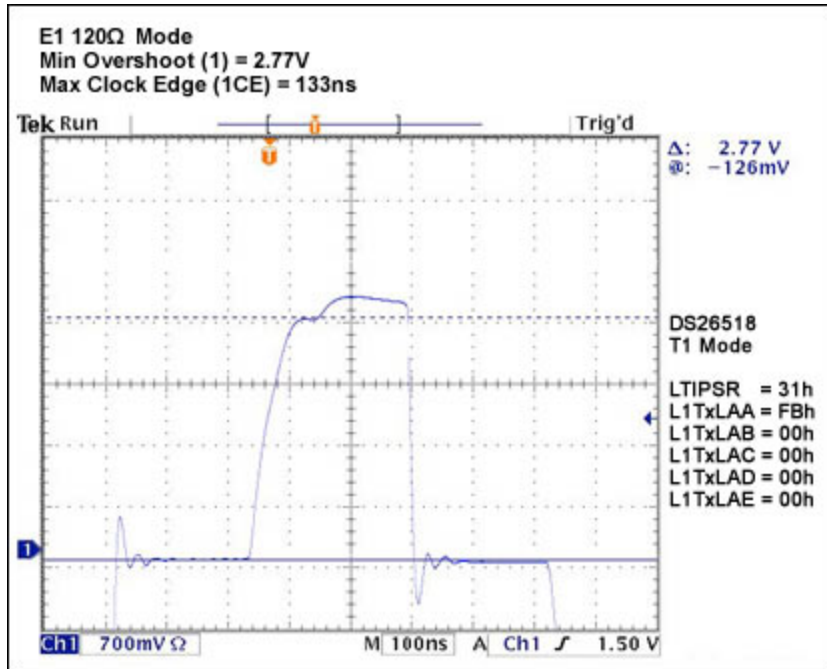


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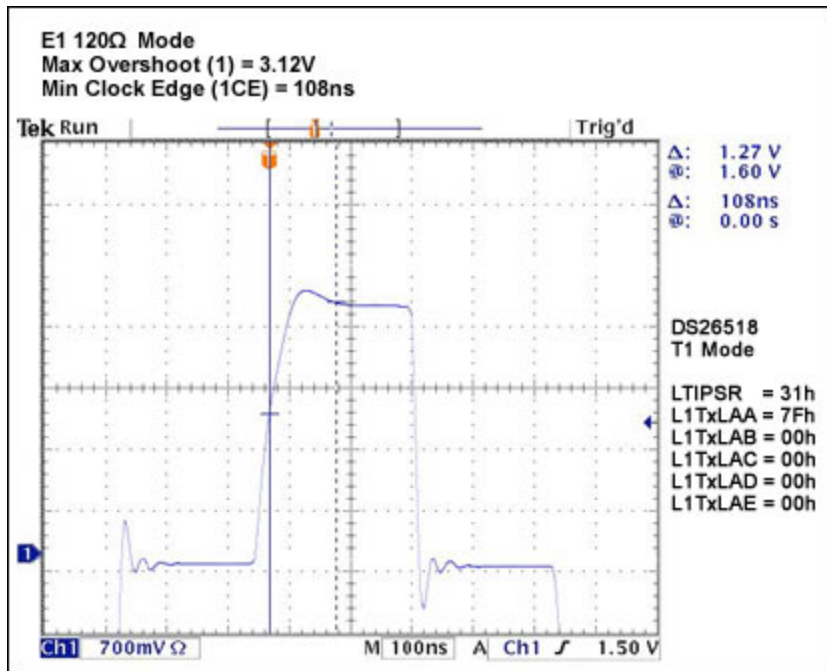


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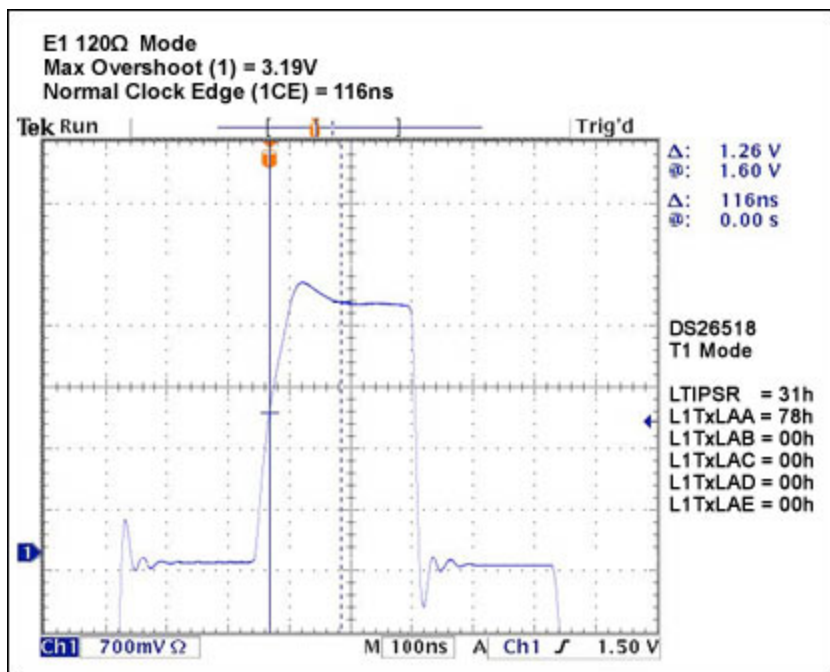


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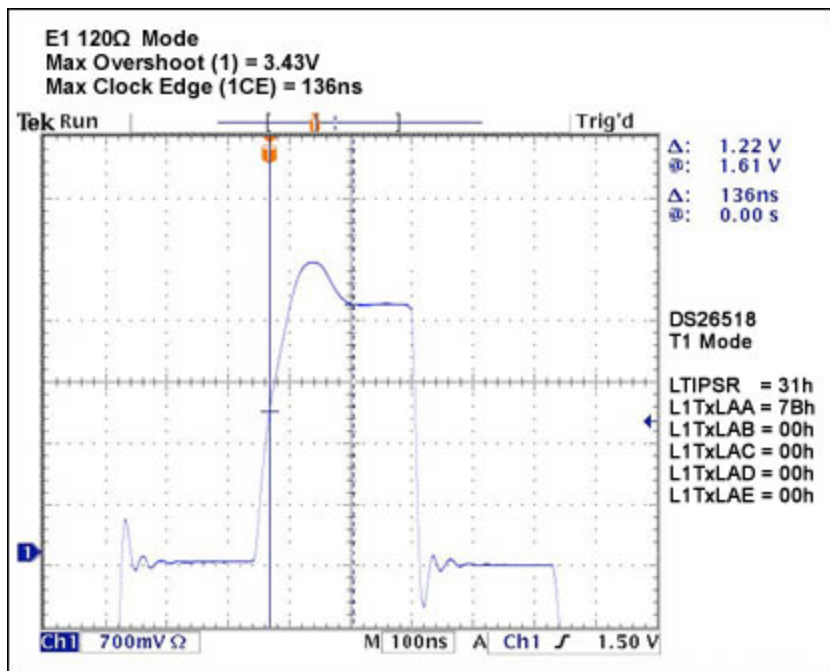


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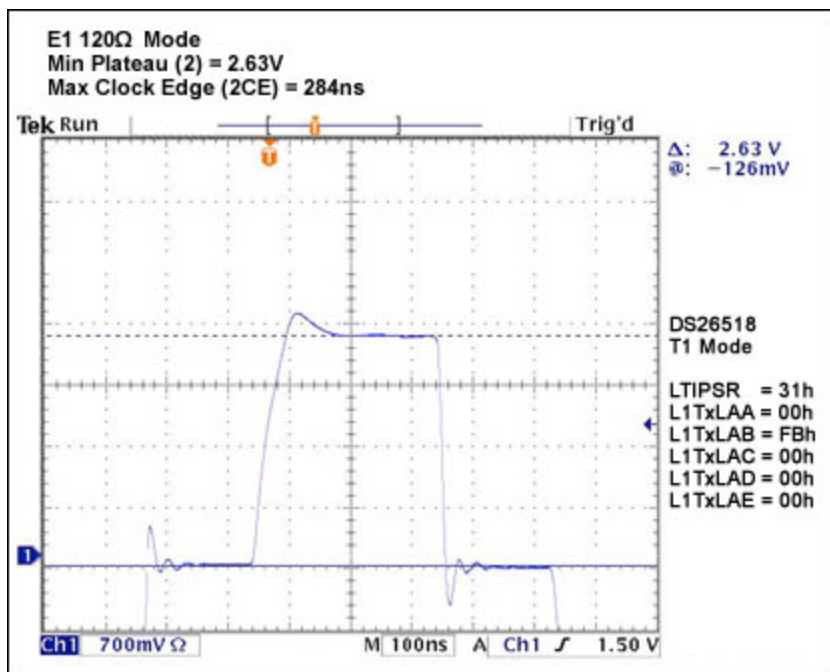


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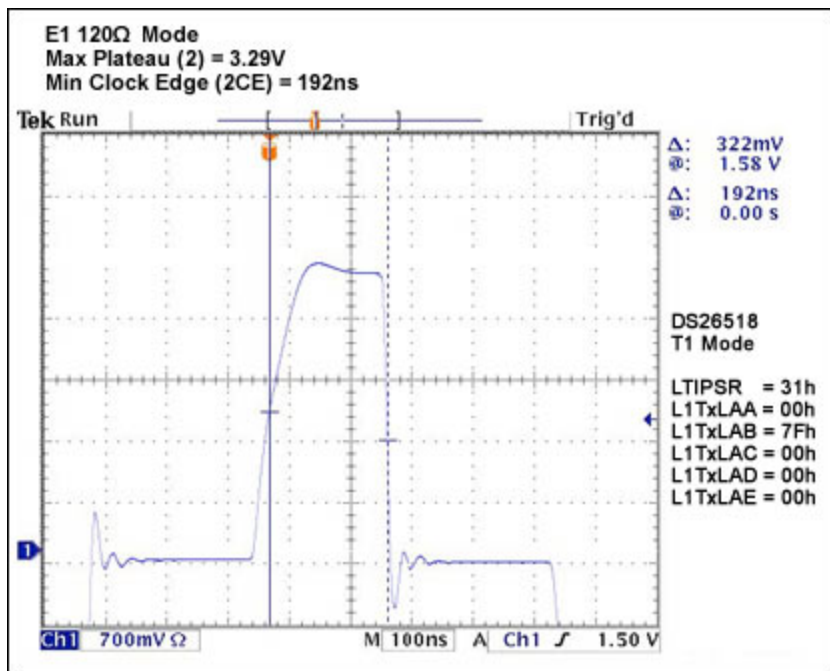


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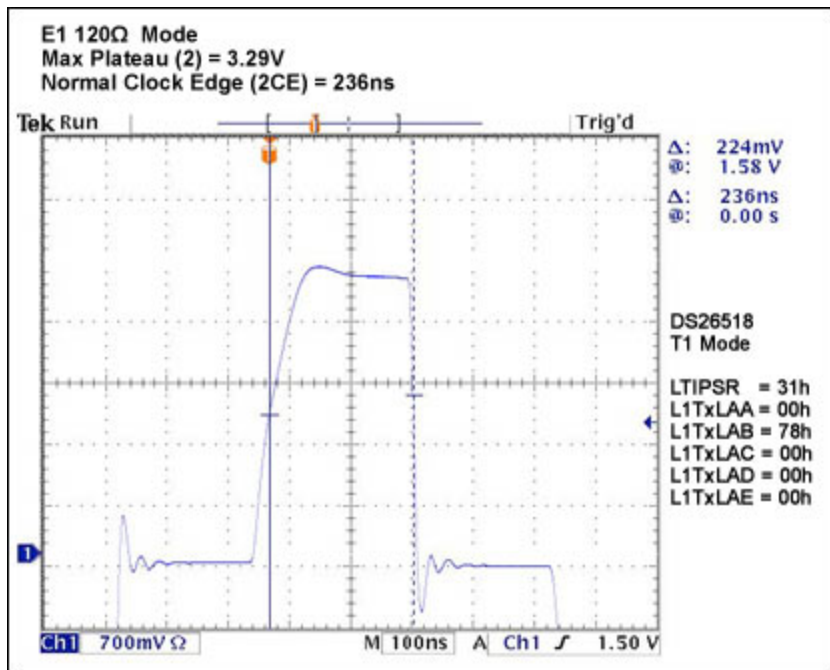


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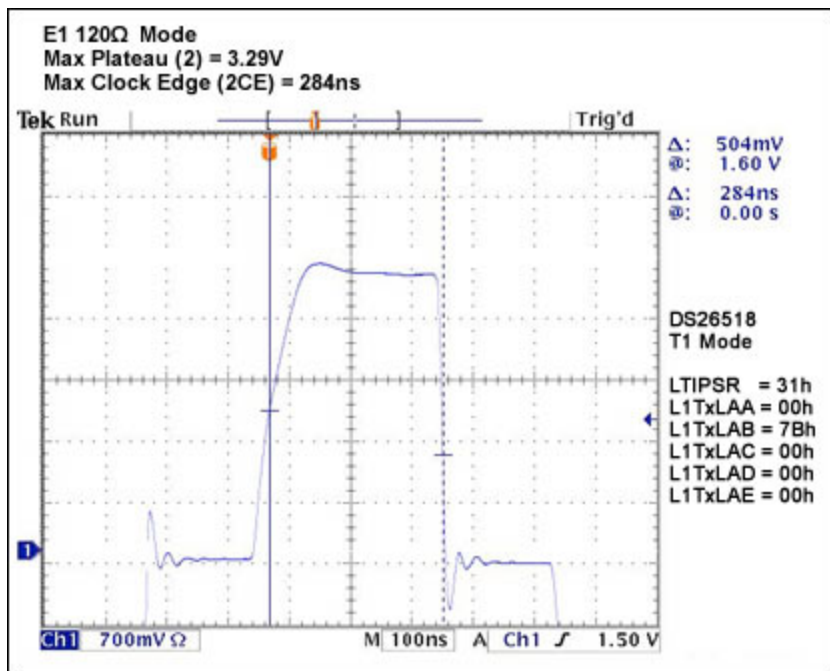


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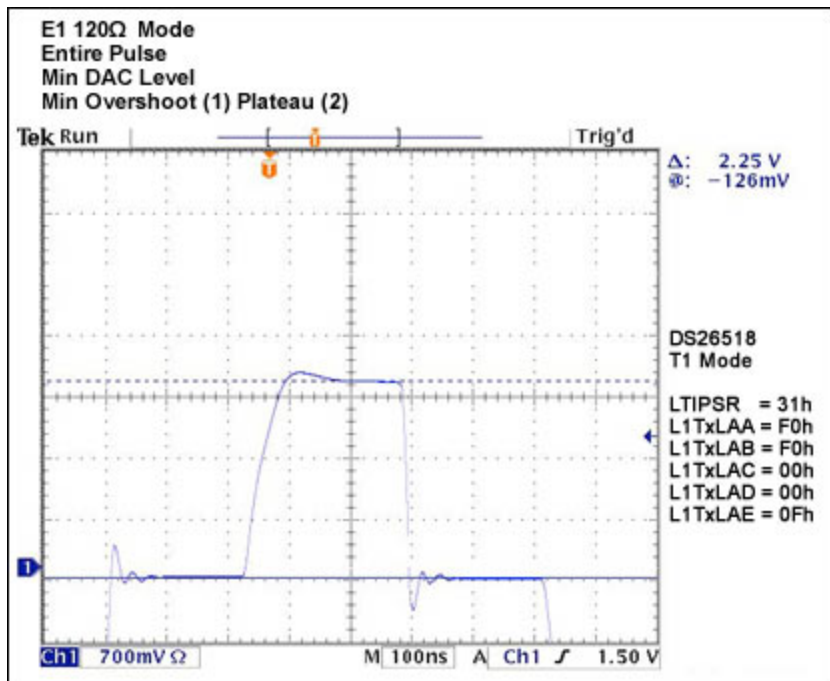


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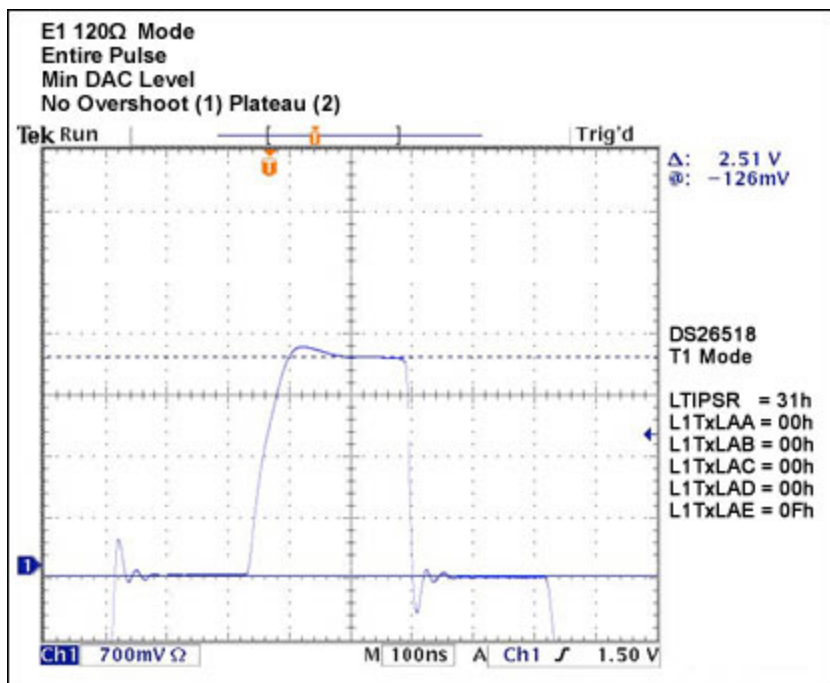


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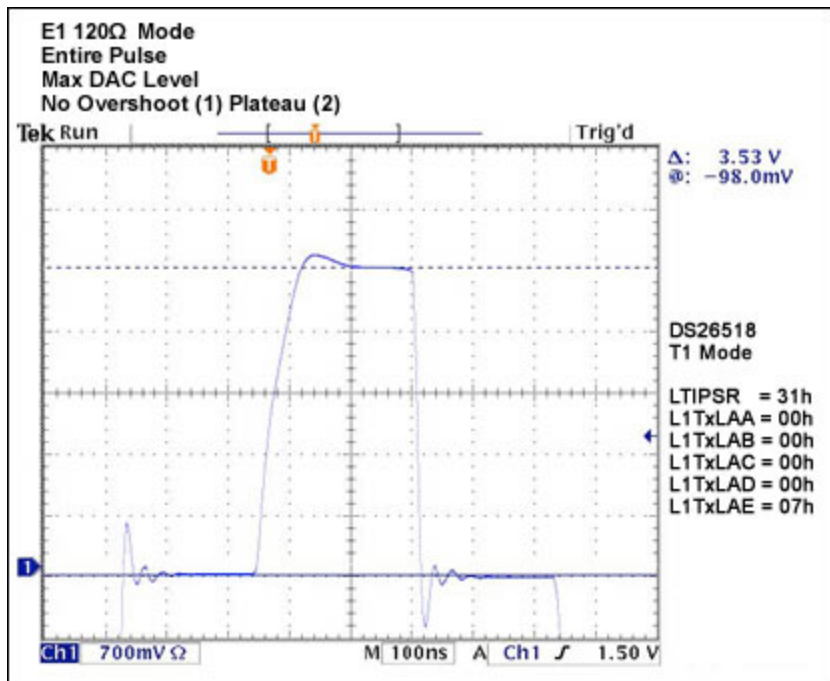


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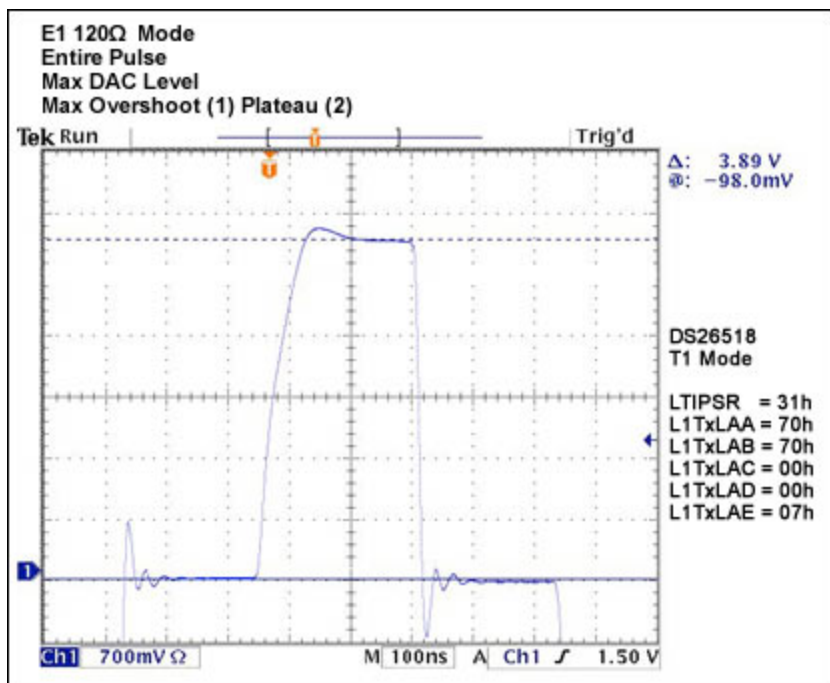


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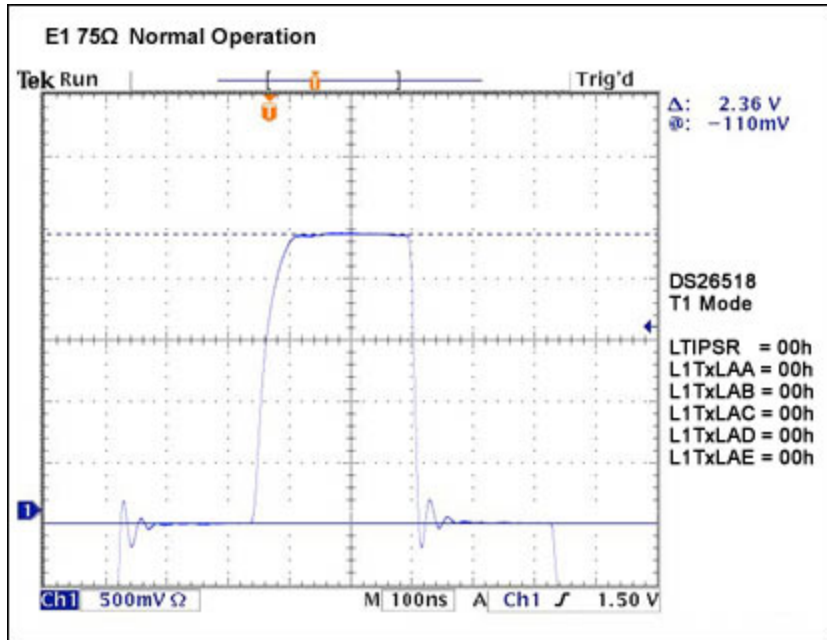


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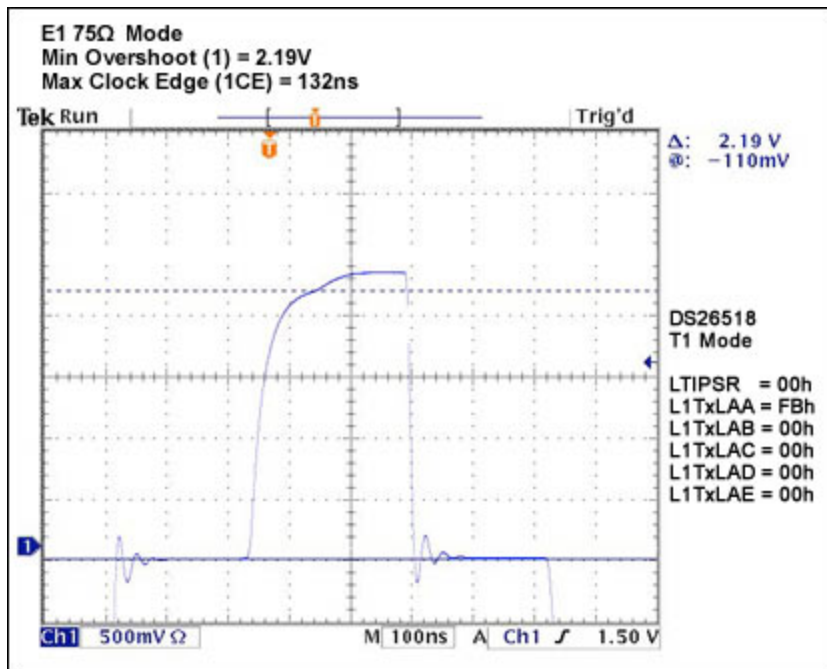


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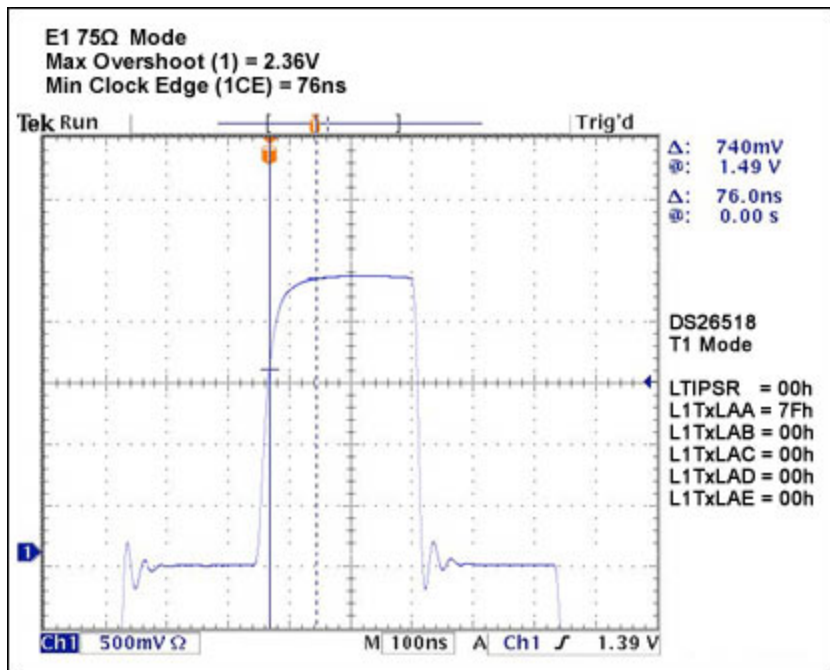


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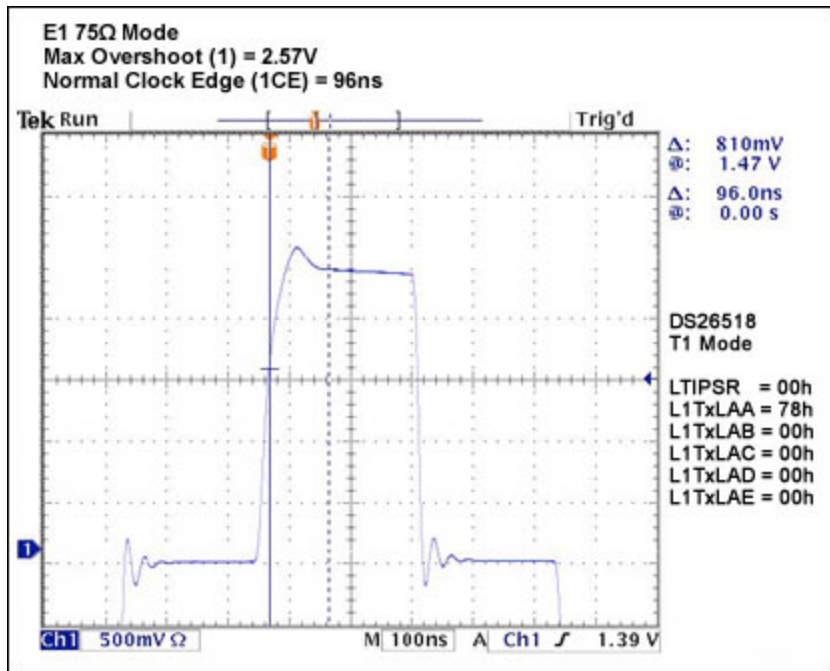


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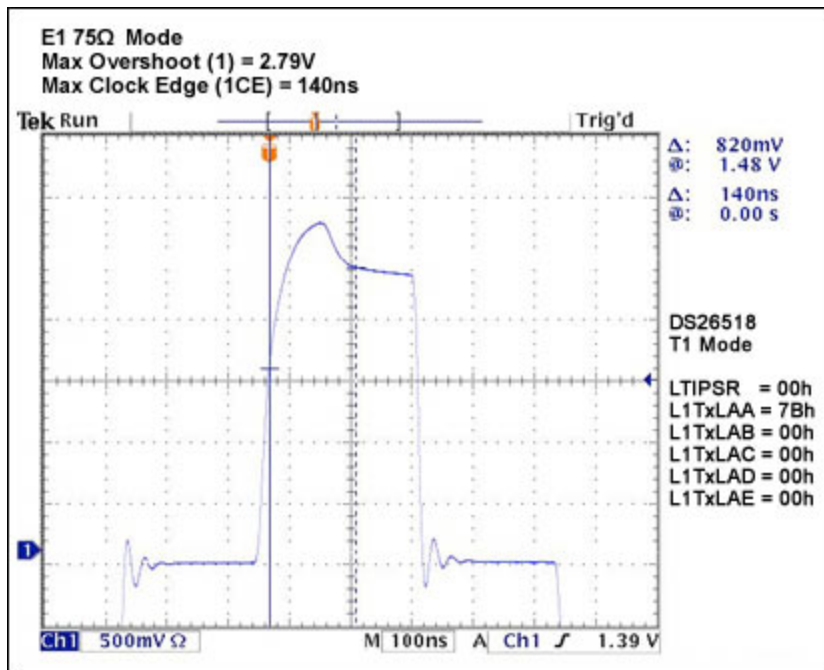


Figure 43.

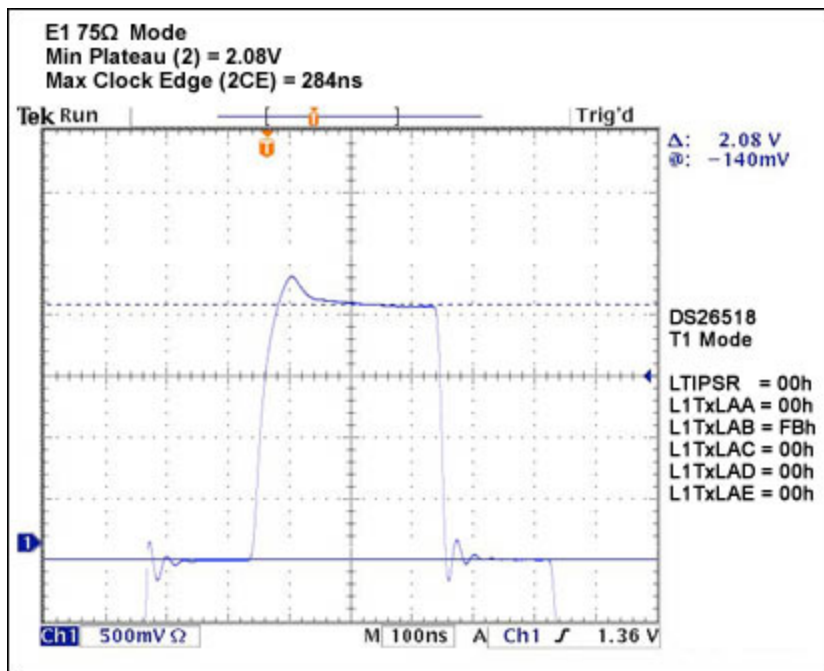


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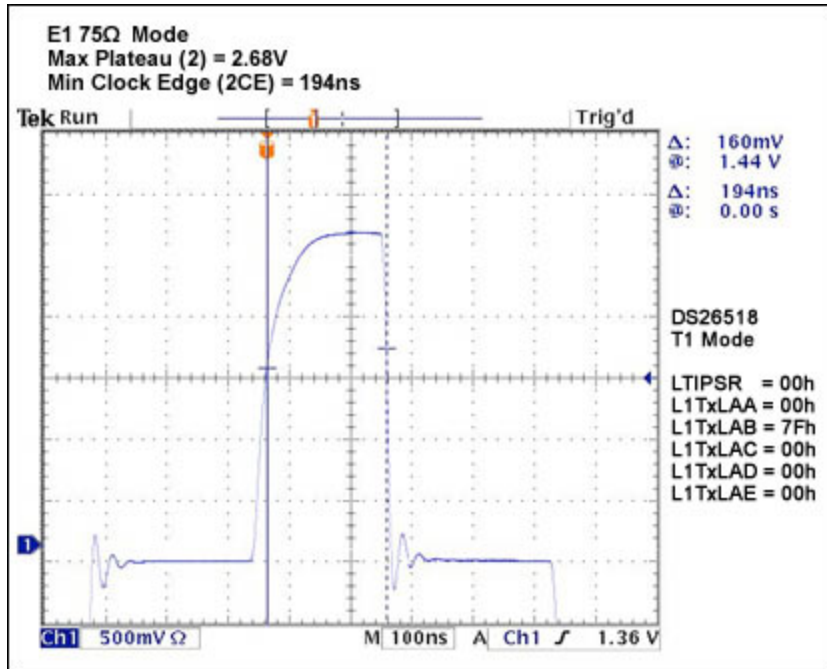


Figure 45.

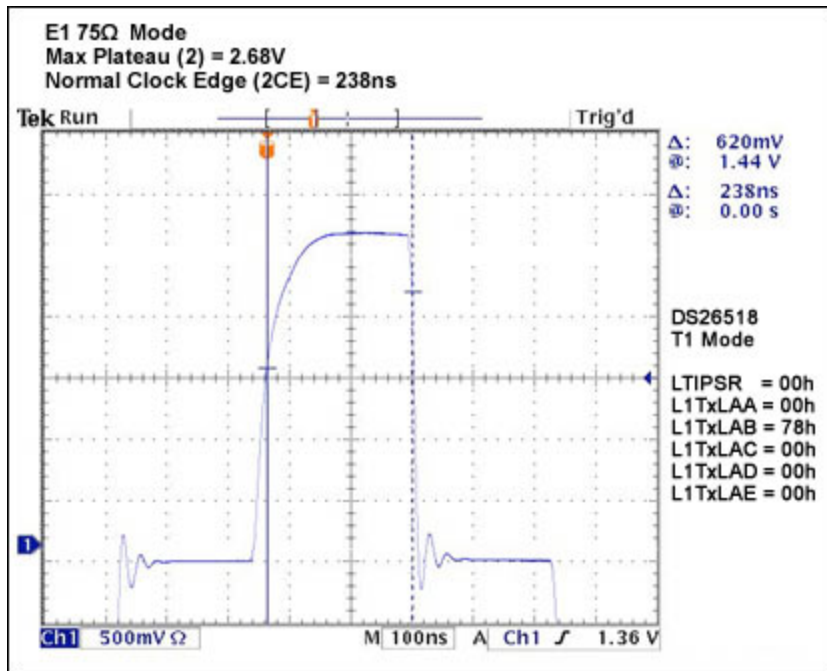


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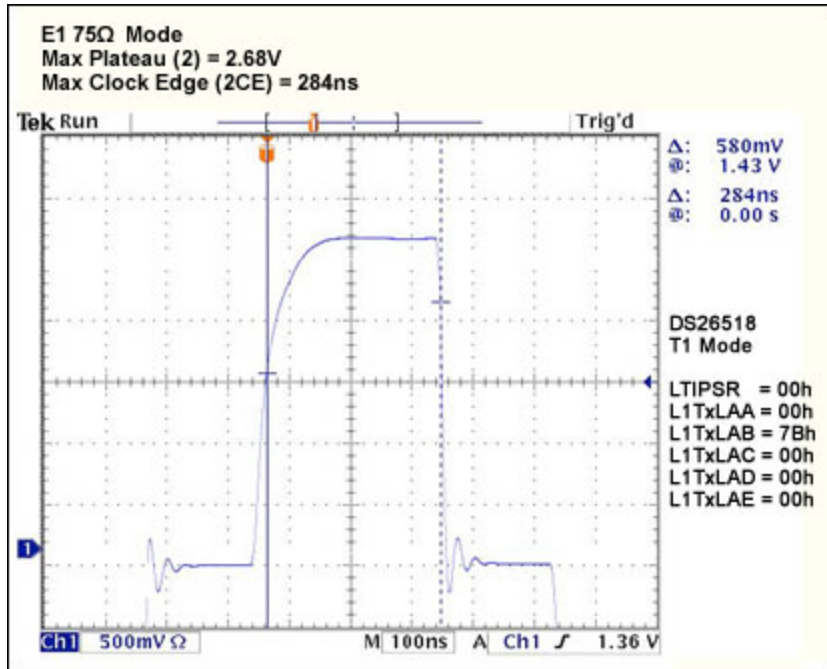


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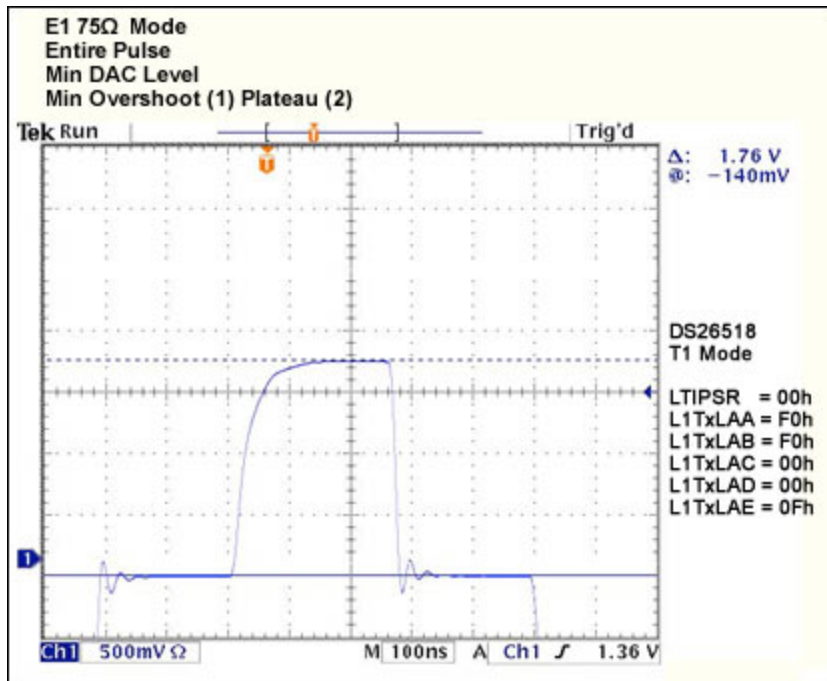


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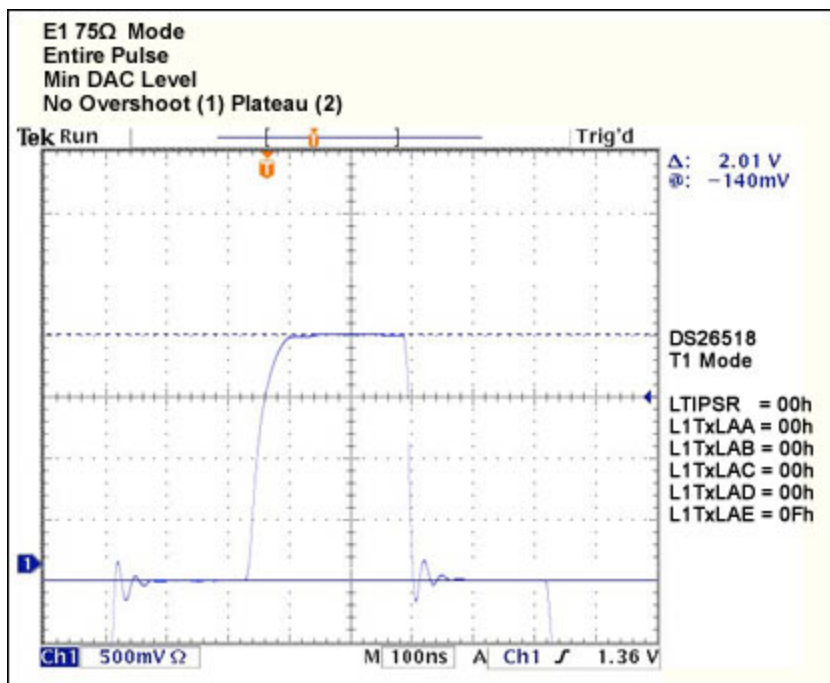


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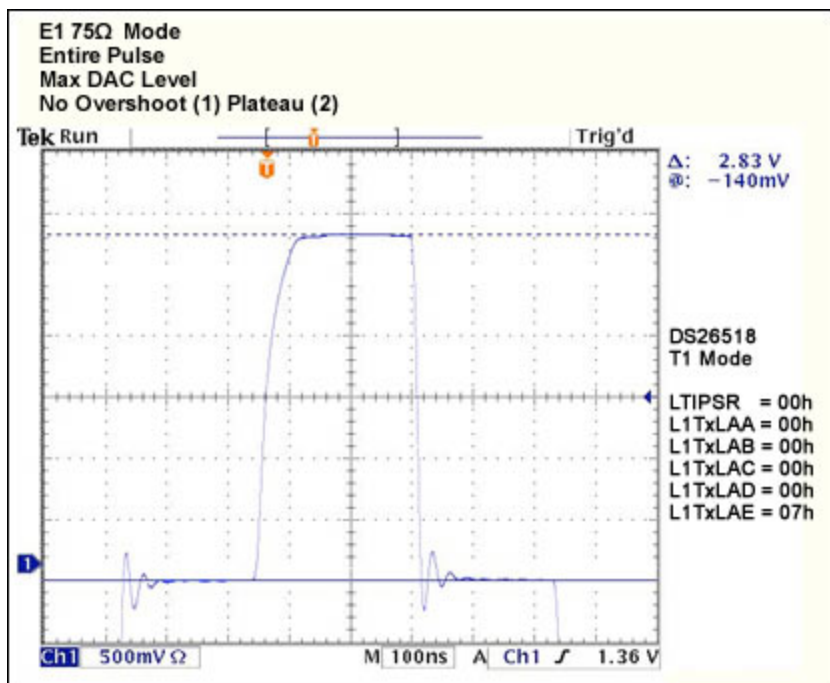


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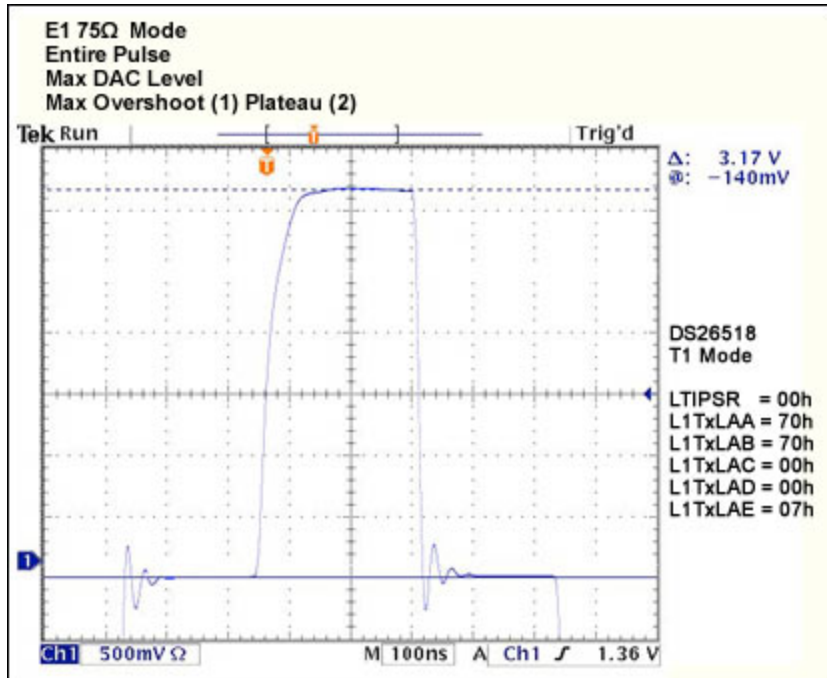


Figure 51.

#### Related Parts

DS26518

8-Port T1/E1/J1 Transceiver

[Free Samples](#)

#### More Information

For Technical Support: <http://www.maximintegrated.com/support>

For Samples: <http://www.maximintegrated.com/samples>

Other Questions and Comments: <http://www.maximintegrated.com/contact>

Application Note 4325: <http://www.maximintegrated.com/an4325>

APPLICATION NOTE 4325, AN4325, AN 4325, APP4325, Appnote4325, Appnote 4325

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