

MC74VHC1G09

2-Input AND Gate with Open Drain Output

The MC74VHC1G09 is an advanced high speed CMOS 2-input AND gate with open drain output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V and when the output voltage exceeds V_{CC} . These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Designed for 2.0 V to 5.5 V V_{CC} Operation
- 4.3 ns t_{PD} at 5 V (typ)
- Inputs/Outputs Over-Voltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 8 mA at 3.0 V
- Available in SC-88A, SC-74A, TSOP-5, SOT-553, SOT-953 and UDFN6 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

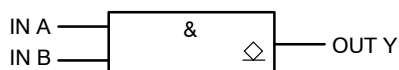

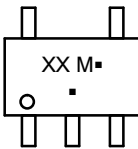

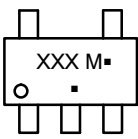

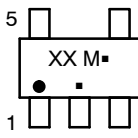



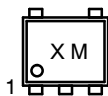






Figure 1. Logic Symbol



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MARKING DIAGRAMS		
	SC-88A DF SUFFIX CASE 419A	
	SC-74A DBV SUFFIX CASE 318BQ	
	TSOP-5 DT SUFFIX CASE 483	
	SOT-553 XV5 SUFFIX CASE 463B	
	SOT-953 P5 SUFFIX CASE 527AE	
	UDFN6 1.45 x 1.0 CASE 517AQ	
	UDFN6 1.0 x 1.0 CASE 517BX	

XX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

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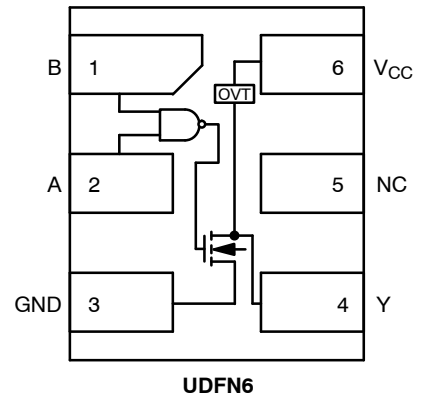
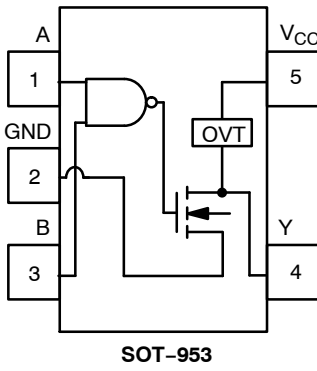
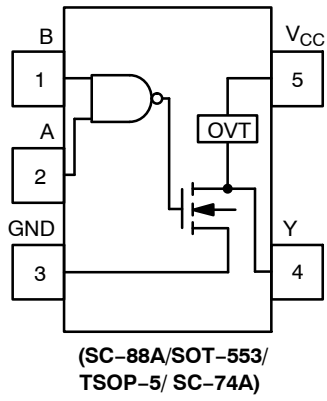


Figure 2. Pinout (Top View)

PIN ASSIGNMENT

(SC-88A/SOT-553/ TSOP-5/SC-74A)

Pin	Function
1	B
2	A
3	GND
4	Y
5	V _{CC}

PIN ASSIGNMENT (SOT-953)

Pin	Function
1	A
2	GND
3	B
4	Y
5	V _{CC}

PIN ASSIGNMENT (UDFN)

Pin	Function
1	B
2	A
3	GND
4	Y
5	NC
6	V _{CC}

FUNCTION TABLE

Input		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	Z

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MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V_{CC}	DC Supply Voltage TSOP-5, SC-88A (NLV) SC-74A, SC-88A, UDFN6, SOT-553, SOT-953	-0.5 to +7.0 -0.5 to +6.5	V
V_{IN}	DC Input Voltage TSOP-5, SC-88A (NLV) SC-74A, SC-88A, UDFN6, SOT-553, SOT-953	-0.5 to +7.0 -0.5 to +6.5	V
V_{OUT}	DC Output Voltage TSOP-5, SC-88A (NLV) Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +7.0 -0.5 to +7.0	V
	DC Output Voltage SC-74A, SC-88A, UDFN6, SOT-553, SOT-953 Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-20	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	+20	mA
I_{OUT}	DC Output Source/Sink Current	+25	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	+50	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2) SC-88A SC-74A TSOP-5 SOT-553 SOT-953 UDFN6	659 555 555 562 560 382	°C/W
P_D	Power Dissipation in Still Air SC-88A SC-74A TSOP-5 SOT-553 SOT-953 UDFN6	190 225 225 222 223 327	mW
MSL	Moisture Sensitivity	Level 1	-
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage TSOP-5, SC-88A (NLV)	0	V _{CC}	V
	DC Output Voltage SC-74A, SC-88A, UDFN6, SOT-553, SOT-953 Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V _{CC} = 0 V)	0	V _{CC}	
		0	5.5	
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time TSOP-5, SC-88A (NLV) V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	0	100	ns/V
		0	20	
	Input Rise and Fall Time SC-74A, SC-88A, UDFN6, SOT-553, SOT-953 V _{CC} = 1.65 V to 1.95 V V _{CC} = 2.3 V to 2.7 V V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	0	20	
		0	20	
		0	10	
		0	5	
		0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (MC74VHC1G09)

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0	1.5	-	-	1.5	-	1.5	-	V
			3.0	2.1	-	-	2.1	-	2.1	-	
			4.5	3.15	-	-	3.15	-	3.15	-	
			5.5	3.85	-	-	3.85	-	3.85	-	
V _{IL}	Low-Level Input Voltage		2.0	-	-	0.5	-	0.5	-	0.5	V
			3.0	-	-	0.9	-	0.9	-	0.9	
			4.5	-	-	1.35	-	1.35	-	1.35	
			5.5	-	-	1.65	-	1.65	-	1.65	
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA I _{OL} = 8 mA	2.0	-	0.0	0.1	-	0.1	-	0.1	V
			3.0	-	0.0	0.1	-	0.1	-	0.1	
			4.5	-	0.0	0.1	-	0.1	-	0.1	
			3.0	-	-	0.36	-	0.44	-	0.52	
			4.5	-	-	0.36	-	0.44	-	0.52	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	-	-	±0.1*	-	±1.0	-	±1.0	μA
I _{OZ}	3-State Output Leakage Current	V _{OUT} = 0 V to 5.5 V	5.5	-	-	±0.25	-	±2.5	-	±2.5	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0	-	-	1.0	-	10	-	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	-	-	1.0	-	20	-	40	μA

*Guaranteed by design.

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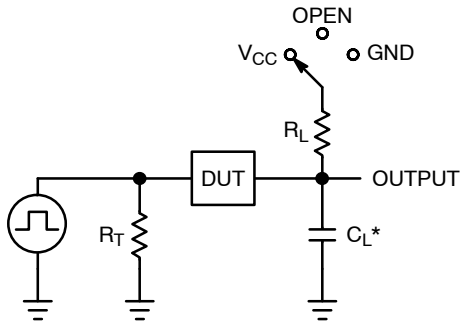
AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PZL}	Output Enable Time, OE to Y (Figures 3 and 4)	C _L = 15 pF	3.0 to 3.6	-	6.2	8.8	-	10.5	-	12.5	ns
				C _L = 50 pF	-	8.7	12.3	-	14.0	-	
		C _L = 15 pF	4.5 to 5.5	-	4.3	5.9	-	7.0	-	9.0	
				C _L = 50 pF	-	5.8	7.9	-	9.0	-	
t _{PLZ}	Output Disable Time, OE to Y (Figures 3 and 4)	C _L = 15 pF	3.0 to 3.6	-	6.5	9.7	-	11.5	-	14.5	ns
				C _L = 50 pF	-	8.7	12.3	-	14.0	-	
		C _L = 15 pF	4.5 to 5.5	-	4.8	6.8	-	8.0	-	10.0	
				C _L = 50 pF	-	5.8	7.9	-	9.0	-	
C _{IN}	Input Capacitance			-	4.0	10	-	10	-	10	pF
C _{OUT}	Output Capacitance	Output in High Impedance State		-	6.0	-	-	-	-	-	pF

C _{PD}	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		8.0	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

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C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Figure 3. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X = Don't Care



Figure 4. Switching Waveforms

V_{CC} , V	V_{mi} , V	V_{mo} , V		V_Y , V
		t_{PLH} , t_{PHL}	t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}	
3.0 to 3.6	$V_{CC}/2$	$(V_{OH} - V_{OL})/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$(V_{OH} - V_{OL})/2$	$V_{CC}/2$	0.3

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ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
MC74VHC1G09DFT1G	SC-88A	VX	Q2	3000 / Tape & Reel
MC74VHC1G09DFT2G	SC-88A	VX	Q4	3000 / Tape & Reel
NLVVHC1G09DFT1G*	SC-88A	VX	Q2	3000 / Tape & Reel
NLVVHC1G09DFT2G*	SC-88A	VX	Q4	3000 / Tape & Reel
MC74VHC1G09DBVT1G (In Development)	SC-74A	TBD	Q4	3000 / Tape & Reel
MC74VHC1G09DTT1G	TSOP-5	VX	Q4	3000 / Tape & Reel
NLV74VHC1G09DTT1G*	TSOP-5	VX	Q4	3000 / Tape & Reel
MC74VHC1G09XV5T2G (In Development)	SOT-553	TBD	Q4	3000 / Tape & Reel
MC74VHC1G09P5T5G (In Development)	SOT-953	TBD	Q2	4000 / Tape & Reel
MC74VHC1G09MU1TCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
MC74VHC1G09MU3TCG (In Development)	UDFN6, 1.0 x 1.0, 0.35	TBD	Q4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel

Direction of Feed



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PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L



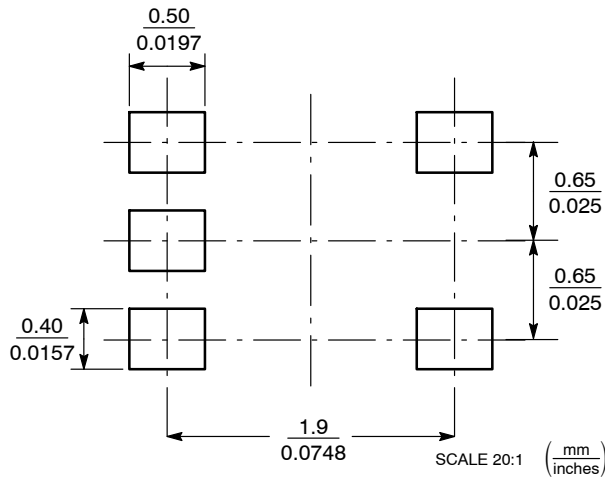
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



SOLDER FOOTPRINT*

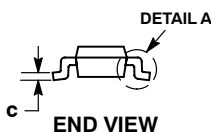
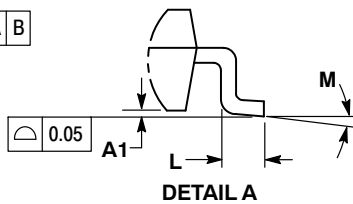
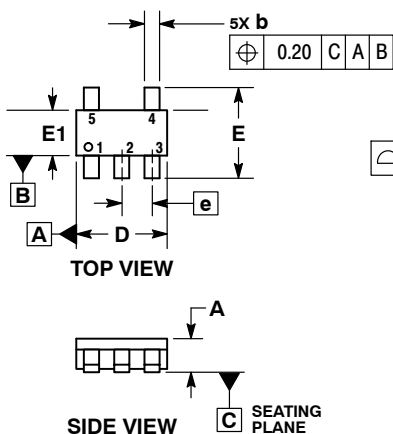


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

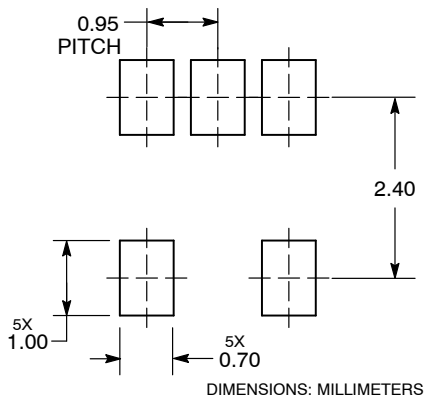
SC-74A
CASE 318BQ
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0° 10°	

RECOMMENDED SOLDERING FOOTPRINT*



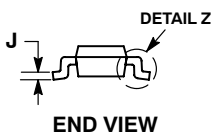
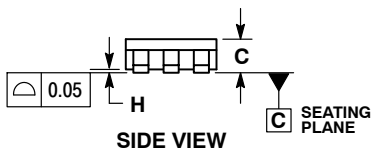
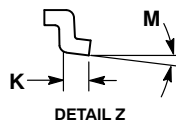
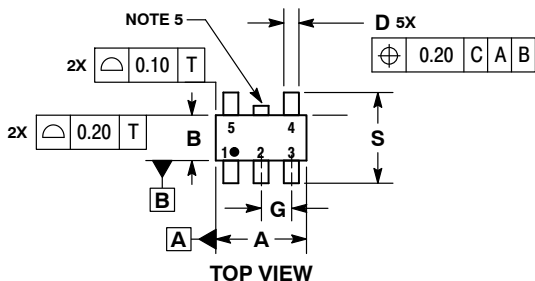
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSOP-5
CASE 483-02
ISSUE M

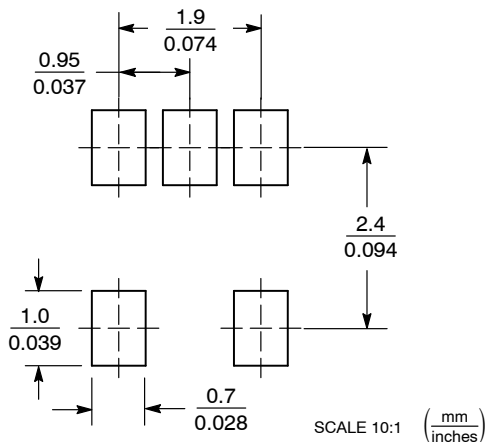


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

MILLIMETERS		
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0° 10°	
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOT-553, 5 LEAD
CASE 463B
ISSUE C

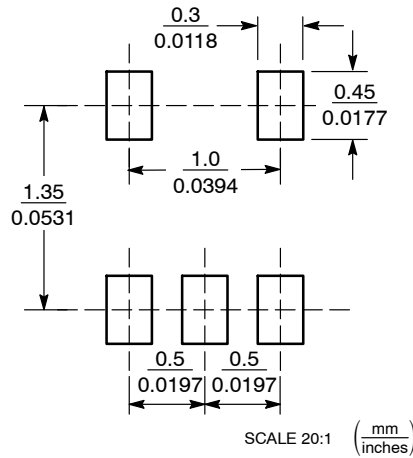


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.55	1.60	1.65	0.061	0.063	0.065

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC1G09

PACKAGE DIMENSIONS

SOT-953
CASE 527AE
ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H _E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

SOLDERING FOOTPRINT*



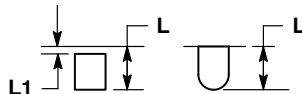
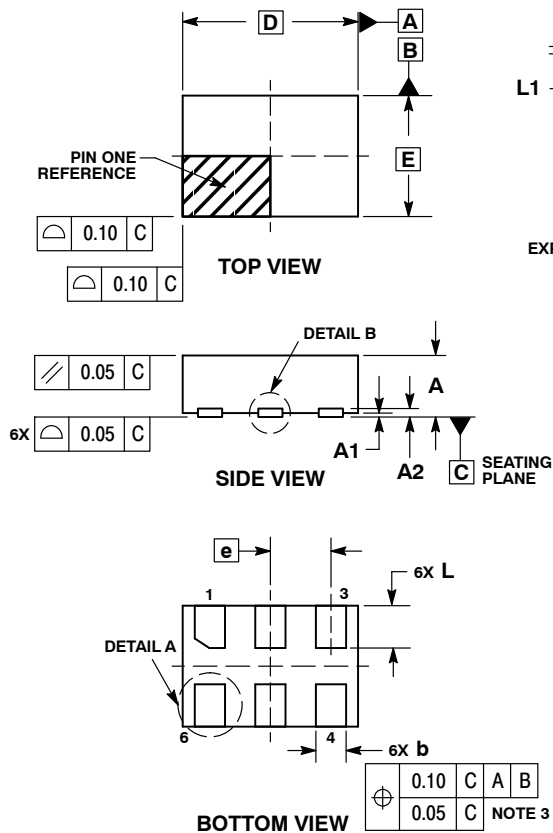
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDETRM/D.

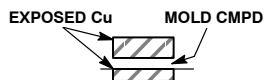
MC74VHC1G09

PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O



DETAIL A
OPTIONAL
CONSTRUCTIONS



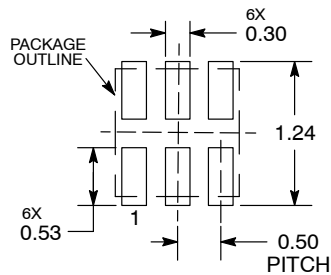
DETAIL B
OPTIONAL
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT



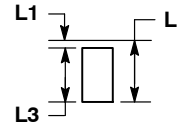
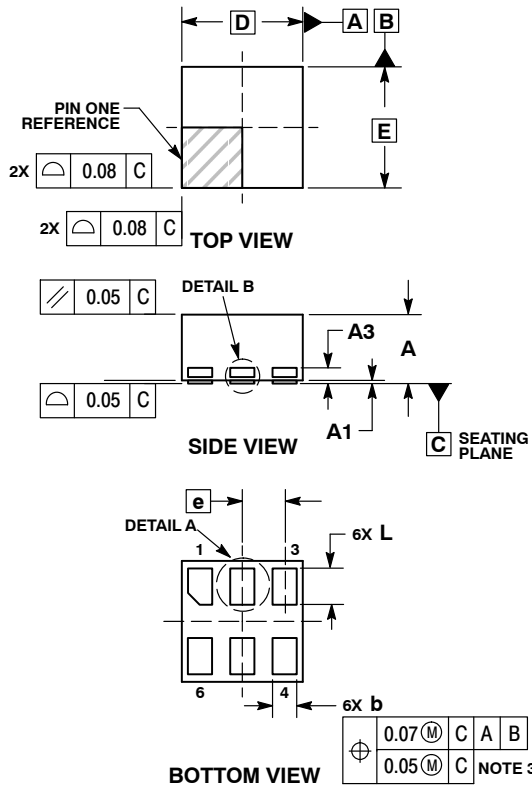
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC1G09

PACKAGE DIMENSIONS

UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.50	0.65
A1	0.00	0.05
A3	0.13	REF
b	0.17	0.23
D	1.00	BSC
E	1.00	BSC
e	0.35	
L	0.20	0.40
L1	---	0.15
L3	0.26	0.33

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

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