Step-Down DC-DC Controller with Remote Sense

General Description

The RT2702 is a high-efficiency and high-current synchronous buck controller designed to drive a DrMOS module. A COT (Constant-On-Time) PWM controller and PWM signal for DrMOS are integrated so that the external circuit is easily designed and the component count is reduced. The RT2702 adopts FCOT control technology that responds instantly to input voltage change. Besides, the RT2702 includes a 5V (VDRV) linear regulator, which can provide 5V voltage and supply up to 100mA for DrMOS.

The RT2702 supports two modes transition function with various operating states, which include audio skipping mode (ASM) and forced-CCM mode (FCCM).

Other features include power good indication, external soft-start setting, soft-off discharge function, precise DCR sense, enable/disable control, over-voltage protection (OVP), under-voltage protection (UVP), current Limit, thermal shutdown into the WQFN-16L 3x3 package.

Ordering Information

RT2702□□(□)

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

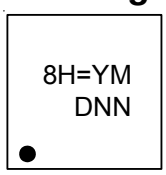
Note :

***Empty means Pin1 orientation is Quadrant 1

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



8H= : Product Code

YMDNN : Date Code

Features

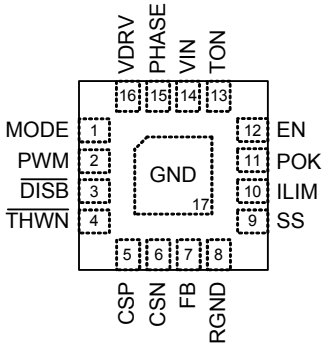
- **4.5V to 19V Input Voltage Range**
- **Adjustable Output Range, 0.6V Reference with 1% Accuracy Over-Temperature Protection**
- **FCOT™ (Flexible Constant On Time) Control**
- **Integrated 5V LDO@100mA for DrMOS module**
- **Support Pre-biased Output**
- **Programmable Soft-Start**
- **Soft-Off through V_{OUT} Discharge**
- **Programmable Switching Frequency**
- **Programmable Over Current Limit**
- **Power Good Indication**
- **OVP, UVP, UVLO Protection**

Applications

- High Current Distributed Power Systems
- Datacom and Telecom Systems
- Industrial Power Supplies

Pin Configuration

(TOP VIEW)

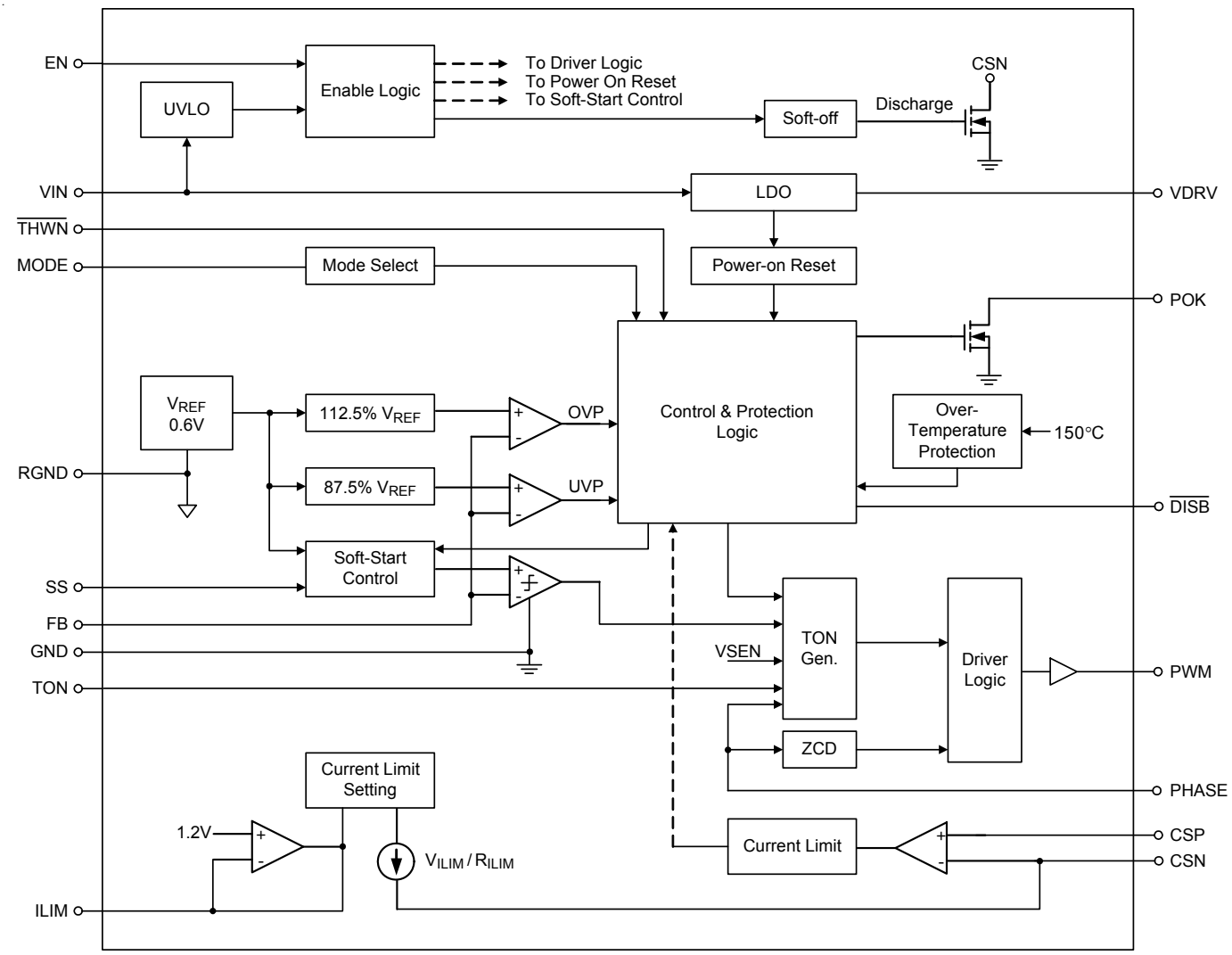


WQFN-16L 3x3

Functional Pin Description

Pin No	Pin Name	Pin Function
1	MODE	Operation mode detection input.
2	PWM	Logic gate driver. This pin provides PWM signal for the gate drive.
3	$\overline{DISB}$	External driver enable. Enable external driver when $\overline{DISB}$ is high, and disable external driver when $\overline{DISB}$ is low.
4	$\overline{THWN}$	Thermal shutdown detection input. $\overline{DISB}$ goes low when $\overline{THWN}$ is less than trip level.
5	CSP	Non-inverting input of current sense amplifier.
6	CSN	Inverting input of current sense amplifier. Connect a R_{CS} from this pin to the current sensing R/C network for adjusting the over current trip threshold. V_{OUT} is also discharged by this pin when system is shut down or any protection is toggled. Resistance of the discharge switch is around 30Ω.
7	FB	Feedback pin. This pin is the negative input node of the PWM comparator.
8	RGND	Remote ground sense. This pin is intended to connect to the negative side of the load for remote sensing.
9	SS	External soft-start pin. Achieve programmable soft-start time function, also have a default internal soft-start time 3ms for minimum soft-start time. DO NOT force this pin lower than 1.2V, otherwise soft-start procedure won't be finished. Refer to “Application Information” for further description.
10	ILIM	The 1.2V buffered output for current limit adjustment. Connect a R_{ILIM} between this pin and GND to set the over-current threshold corresponding to R_{CS}.
11	POK	Open drain power good indicator. High impedance indicates power is good.
12	EN	Enable control input. The device enters its 20μA supply current shutdown mode if EN is less than the EN input falling edge trip level and does not restart until EN is greater than the EN input rising edge trip level. Connect EN to VIN for automatically startup. EN can be connected to VIN through a resistive voltage divider to implement a programmable under-voltage lockout.
13	TON	On-time/switching frequency adjustment input. Connect a resistor to VIN for adjusting switching frequency. And connect an another 100pF ceramic capacitor between TON and ground is optional for noise immunity enhancement.
14	VIN	Power supply input.
15	PHASE	Switching node Input for zero current detection. Also provide V_{OUT} information through PHASE pin to on-time generation circuit.
16	VDRV	Output bypass for the 5V regulator. Connect a low-ESR bypass ceramic capacitor of 4.7μF from this pin to GND.
17 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.

Functional Block Diagram



Operation

The RT2702 includes a constant on-time synchronous step-down controller and a linear regulator.

Buck Controller

In normal operation, the high-side N-MOSFET of DrMOS is turned on when the V_{FB} is lower than V_{REF}, and is turned off after the internal one-shot timer expires. While the high-side N-MOSFET of DrMOS is turned off, the low-side N-MOSFET of that is turned on to conduct the inductor current until next cycle begins.

Soft-Start

For internal soft-start function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval. For external soft-start function, an additional capacitor, connected between SS pin and GND, will be charged by a current source and determines the soft-start time. The RT2702 will track the slower one soft-start ramp during soft-start process.

POK

The power ok is the output of open-drain buffer. When the soft-start process is finished, this pin becomes high impedance.

Current Limit

The current limit circuit employs a unique "valley" current sensing algorithm. If V_{CSP} is higher than V_{CSN}, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current, eventually, output drops lower than the under-voltage protection threshold, inducing IC shutdown.

Over-Voltage Protection (OVP) & Under-Voltage Protection (UVP)

The output voltage is continuously monitored for over-voltage and under-voltage conditions. When the voltage of FB pin exceeds over-voltage threshold (112.5% of V_{REF}), the PWM signal goes low. When it is less than 87.5% of V_{REF}, under-voltage protection is triggered and then the $\overline{DISB}$ signal will be pulled low to disable DrMOS. The controller begins hiccup procedure and restart up after 20ms.

VDRV

Internal LDO turns on When the V_{IN} and EN voltage exceed the POR rising threshold, respectively. Provide 5V supply voltage at VDRV pin.

Absolute Maximum Ratings (Note 1)

- VIN, TON, EN to GND ---------- –0.3V to 20V
- PHASE to GND
  - DC ---------- –0.3V to 20V
  - <100ns ---------- –8V to 30V
- VDRV, MODE, PWM, $\overline{THWN}$, $\overline{DISB}$ to GND ---------- –0.3V to 6V
- CSP, CSN, FB, SS, ILIM, POK to GND ---------- –0.3V to 6V
- RGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  - WQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  - WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - CDM (Charged-Device Model) ---------- 1kV

Recommended Operating Conditions (Note 4)

- Input Supply Voltage, VHV ---------- 4.5V to 19V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = V_{EN} = 6V, R_{TON} = 390kΩ, T_A = –40°C to 105°C , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Operating Conditions						
VIN Voltage Range	V_{IN}		4.5	--	19	V
VIN Supply Current						
VIN Operating Current	I_Q	V_{IN} = 6V, EN = high, V_{FB} = 0.6V	--	--	1	mA
VIN Shutdown Current	I_{SD}	V_{IN} = 6V, EN = low	--	--	40	μA
VIN Supply Voltage						
VIN UVLO Start Threshold	V_{IN_UVLO}	Rising	--	--	4.5	V
VIN UVLO Hysteresis	$V_{IN,UVLO\_HYS}$		--	500	--	mV
VDRV Regulator						
VDRV Output Voltage	V_{DRV}	V_{IN} > 5.5V, I_{VDRV} < 35mA	4.8	5	5.3	V
VDRV Output Voltage		4.5V < V_{IN} < 5.5V, I_{VDRV} < 25mA	4	5	5.3	V
VDRV Output Current	I_{DRV}	V_{DRV} = 4V	100	--	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VREF						
Internal Reference Voltage	V_{REF}	T_A = 25°C	0.597	0.6	0.603	V
Output Voltage Accuracy	ΔV_{FB}	V_{FB} to RGND excluding external resistor divider tolerance	-1	--	1	%
Switching Frequency Control						
Switching Frequency	f_{SW}	V_{IN} = 6V, V_{OUT} = 1V, R_{TON} = 390kΩ	--	500	--	kHz
Minimum Turn Off Time (LG on)	t_{OFF_MIN}	V_{FB} = 0.55V	--	275	400	ns
Minimum Skip Mode Frequency		V_{FB} > 0.6V	20	--	--	kHz
Soft- Start						
Soft Start Setting Current	I_{SS}		8	10	12	μA
Internal Soft Start	t_{SS_INT}	V_{SS} = VDRV, 10% V_{REF} to 90% V_{REF}	1	3	5	ms
Soft- Off						
Soft Off Bleeding Resistor	R_{DIS}		--	30	--	Ω
Over Current Protection						
V_{ILIM} Output Voltage	V_{ILIM}		1.188	1.2	1.212	V
Over Current Threshold Offset	V_{OC_OFS}	$V_{CSP} - V_{CSN} = V_{ILIM}$ x (R_{CS}/R_{ILIM}) = 50mV	–3	--	3	mV
Zero Current Threshold	V_{ZC}	GND – PHASE	–6	--	2	mV
Protection and PGOOD						
POK Output Voltage		Logic low, sinking 4 mA	--	--	0.4	V
OVP Threshold	V_{OVP}	V_{FB} rising	108.5	112.5	116.5	%
UVP Threshold	V_{UVP}	V_{FB} falling	83.5	87.5	91.5	%
Power Good Low Delay	t_{POK_DLY}		--	10	--	μs
PWM Driving Capability						
PWM Source Resistor	R_{PWM_SRC}	V_{DRV} to PWM	--	--	35	Ω
PWM Sink Resistor	R_{PWM_SK}	PWM to GND	--	--	15	Ω
Logic I/O						
EN Input Threshold Voltage	V_{EN_OFF}	Controller OFF	0.8	0.92	1	V
	V_{EN_ON}	Controller ON	0.88	1	1.05	V
MODE Input Voltage	V_{MODE_L}	ASM (Audio Skipping Mode)	--	--	0.4	V
	V_{MODE_H}	FCCM	1.2	--	--	V
$\overline{\text{THWN}}$ Input Voltage	$V_{\overline{THWN}\_L}$	PWM float, VDRV remains ON	--	--	0.4	V
	$V_{\overline{THWN}\_H}$	Normal operation	2	--	--	V
$\overline{\text{DISB}}$ Output Resistor	$V_{\overline{DISB}\_SRC}$	VDRV to $\overline{\text{DISB}}$	--	--	55	Ω
	$V_{\overline{DISB}\_SK}$	$\overline{\text{DISB}}$ to GND	--	--	30	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown						
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	25	--	°C

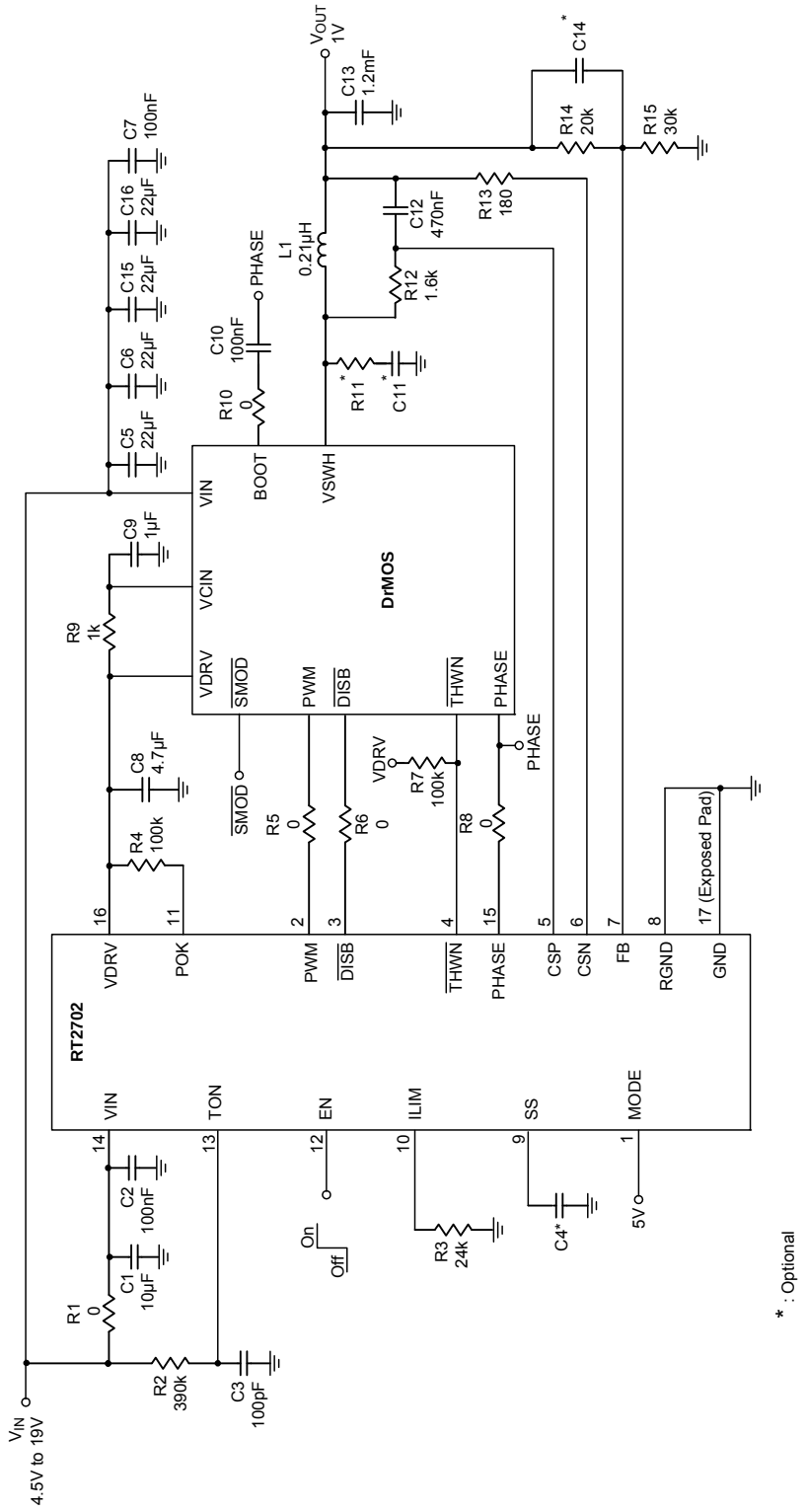
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

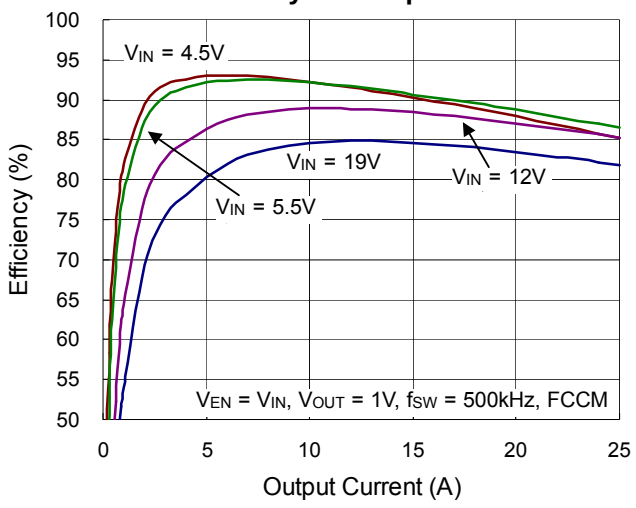
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

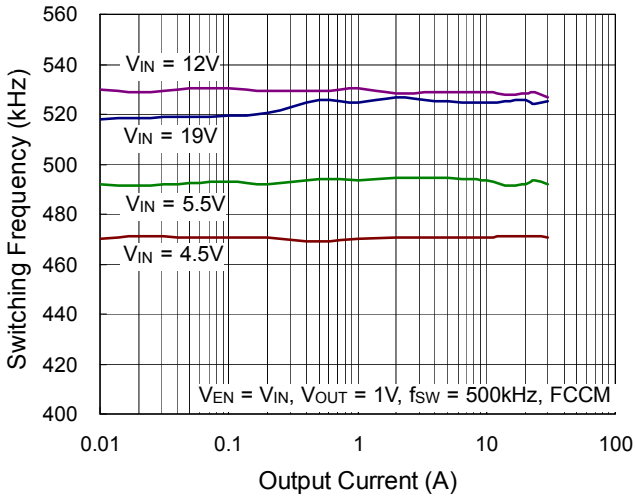


Typical Operating Characteristics

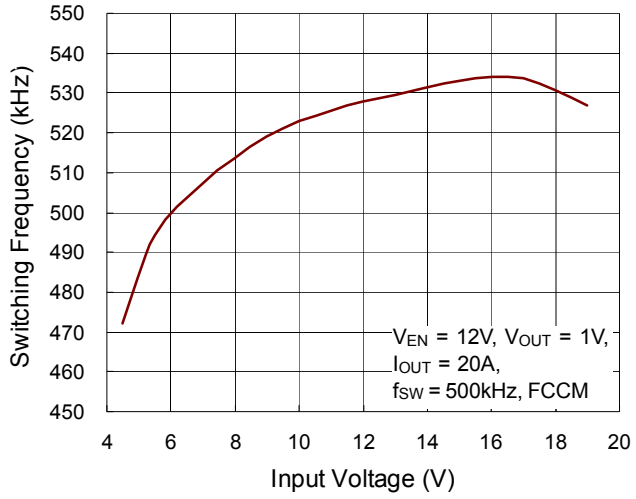
Efficiency vs. Output Current



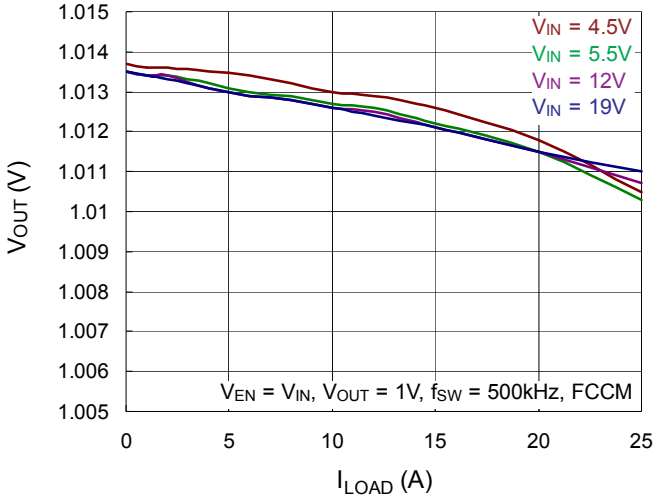
Switching Frequency vs. Output Current



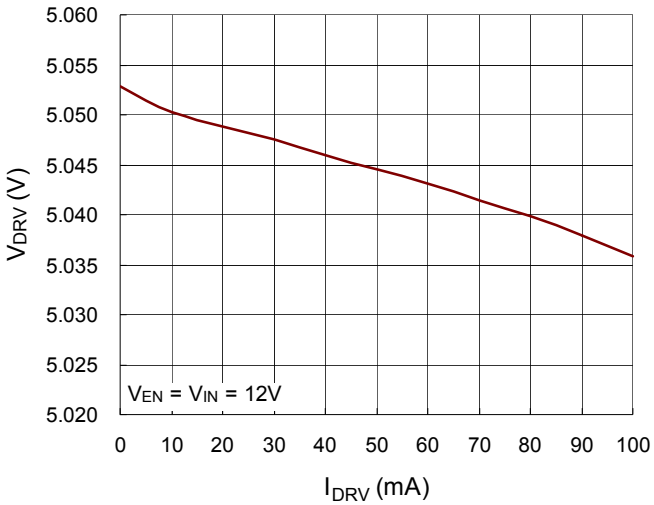
Switching Frequency vs. Input Voltage



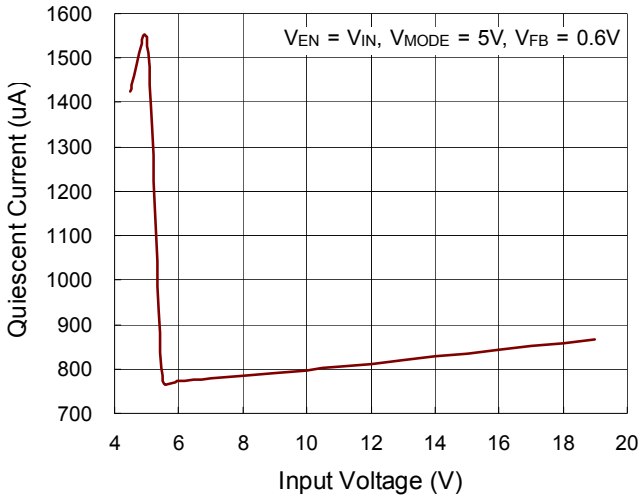
VOUT vs. ILOAD



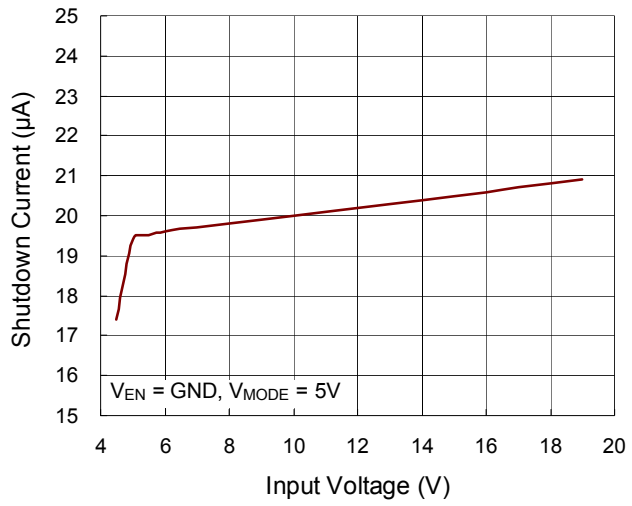
VDRV vs. IDRV



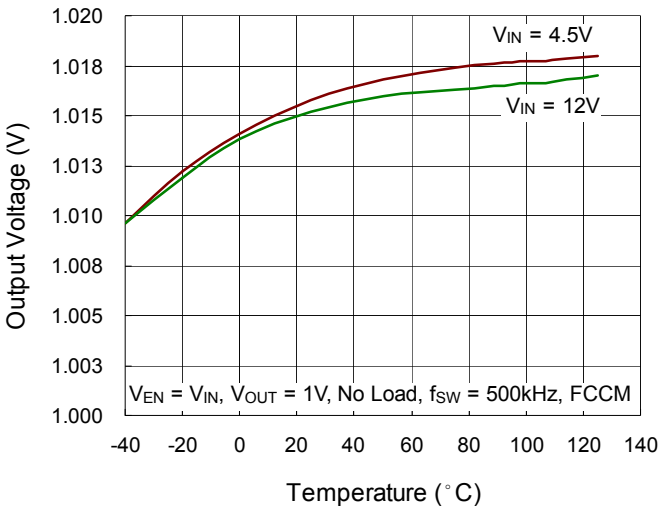
Quiescent Current vs. Input Voltage



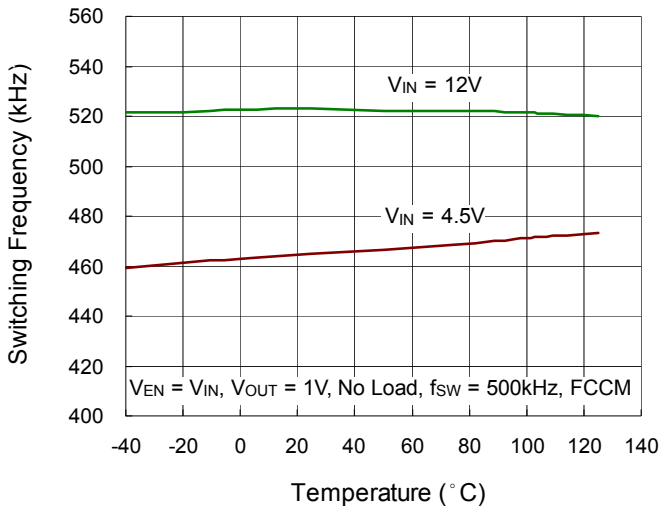
Shutdown Current vs. Input Voltage



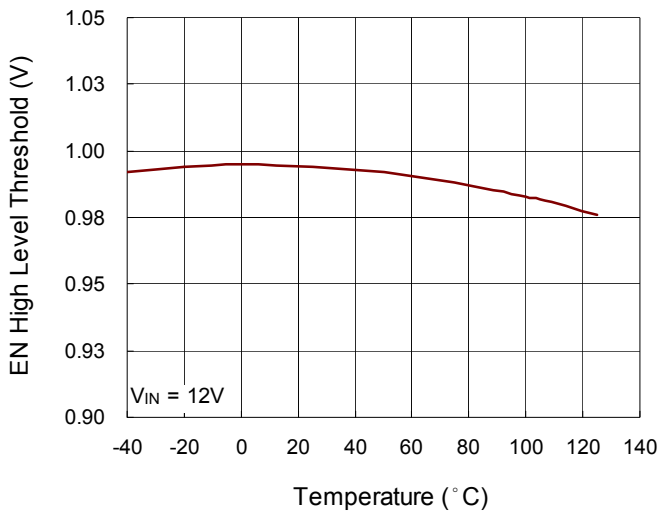
Output Voltage vs. Temperature



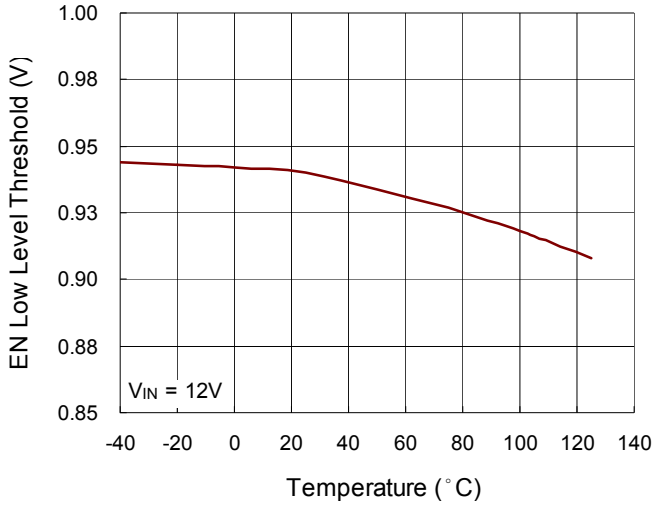
Switching Frequency vs. Temperature



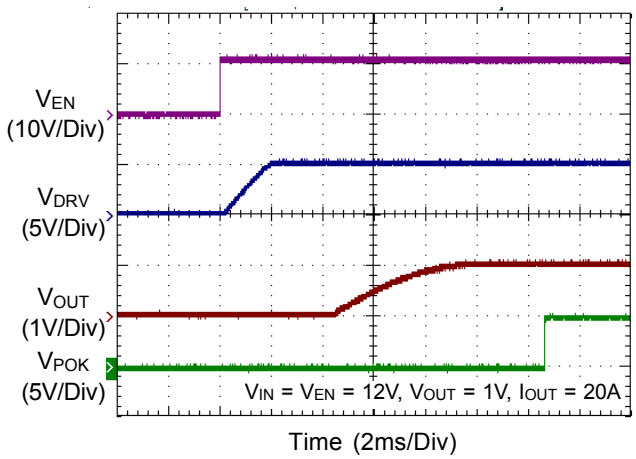
EN High Level Threshold vs. Temperature



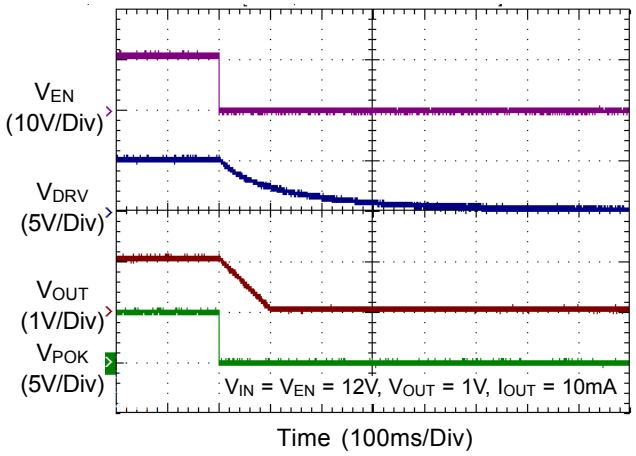
EN Low Level Threshold vs. Temperature



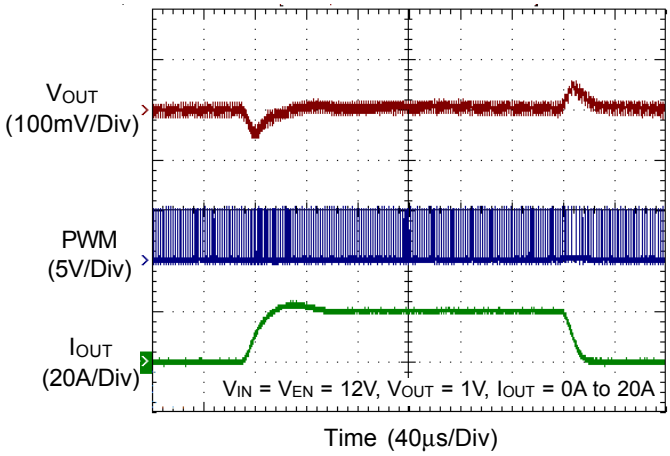
Power On from EN



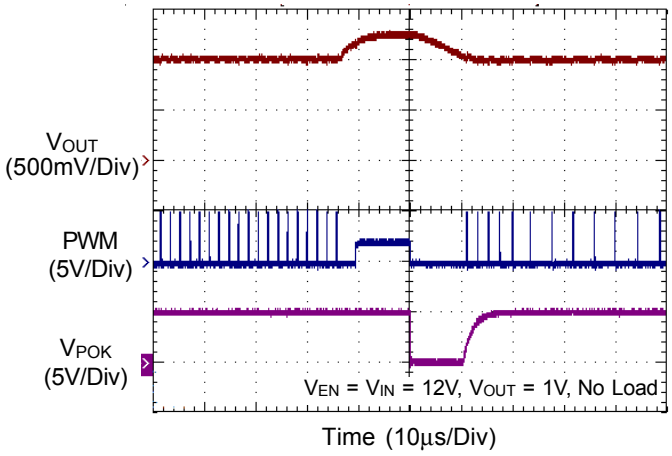
Power Off from EN



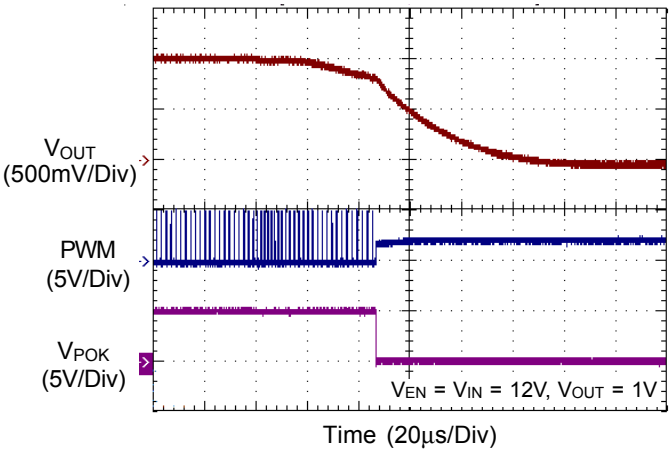
Load Transient Response



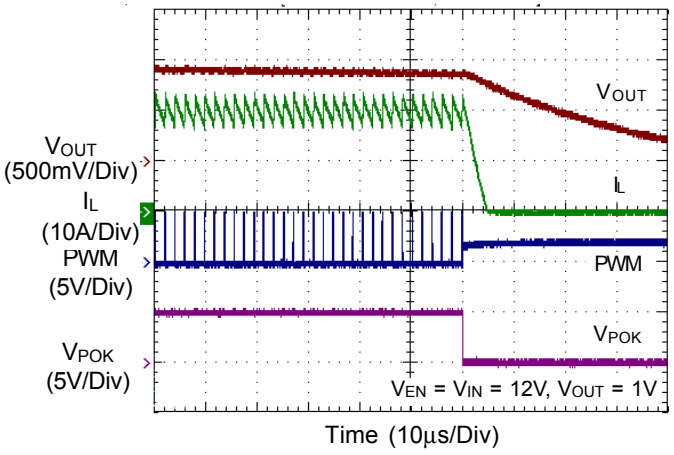
OVP



UVP



Over Current Limit



Application Information

The RT2702 is a high-efficiency and high-current synchronous buck controller designed to drive a DrMOS module. A COT (Constant-On-Time) PWM controller and PWM signal for DrMOS are integrated so that the external circuit is easily designed and the component count is reduced. The RT2702 adopts FCOT control technology that responds instantly to input voltage change. Besides, the RT2702 includes a 5V (VDRV) linear regulator, which can provide 5V voltage and at least 100mA current loading.

The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs while avoiding the problems caused by widely varying switching frequency in conventional constant-on-time and constant-off-time PWM schemes.

The IC supports two modes transition function with various operating states, which include audio skipping mode (ASM) and forced-CCM mode (FCCM). These different operating eliminates audio-frequency modulation and states make the system efficiency as high as possible.

The device can operate at wide input voltage range from 4.5 V to 19V. It is capable of producing an output voltage as low as 0.6V. Other features include power good indication, external soft start setting, soft-off discharge function, OVP, UVP, Current Limit, precise DCR sense, and enable/disable control.

PWM Operation

The RT2702 integrates a Constant-On-Time PWM controller, and the controller provides the PWM signal which relies on the FB voltage comparing with internal reference voltage as shown in Figure 1. Refer to the function block diagram of the RT2702, the synchronous high side MOSFET of DrMOS will be turned on at the beginning of each cycle. After the internal one shot timer expires, the MOSFET will be turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency constant in a specific input voltage range. Another one shot sets a minimum off-time (275ns typ.). The on-time one shot will be triggered if the PWM comparator output is high, the low side switch current is below the current limit threshold and the minimum off-time one shot has timed out.

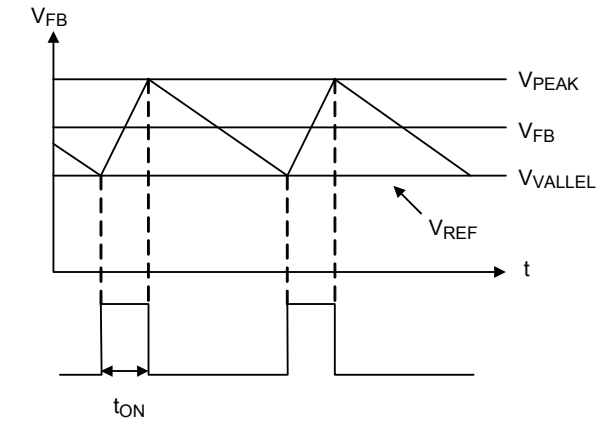


Figure 1. Constant On-Time PWM Control

On-Time Control

A resistor, R_{TON}, is connected between VIN and TON generates on-time current forward to TON Gen. block. With different VIN voltage and R_{TON} value, the on-time current has different value. This on-time current charges an internal capacitor, C_{TON}, which is about 3.8pF, then the on-time will be the voltage on C_{TON} from 0V to V_{OUT}. Besides, the switching frequency, f_{SW}, is roughly determined by R_{TON} and C_{TON} without a clock generator.

$$t_{ON} = \frac{R_{TON} \times V_{OUT} \times 3.8p}{V_{IN} - 1.17}$$

And the specific switching frequency f_{SW} is :

$$f_{SW} = \frac{V_{OUT}}{V_{IN} \times t_{ON}}$$

The recommended operating frequency is between 200kHz and 1.2MHz.

Mode Selection

The RT2702 operates under audio skipping mode (ASM) or force-CCM (FCCM) according to MODE pin voltage setting. If MODE voltage is pulled below 0.4V, controller turns on ASM function. If MODE voltage is higher than 1.2V, controller enters forced-CCM.

Audio Skipping Mode (ASM)

The RT2702 activates a unique type of diode emulation mode with switching frequency of 30kHz, called audio skipping mode. This mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In audio skipping mode, if the PWM switching frequency is lower than 30kHz, controller will force PWM go low to turn on low-side switch of DrMOS. When FB is discharged to V_{REF}, then a regular PWM pair is generated. Thus, the sequence of PWM signal would be HiZ-state, low-state, high-state, low-state, and back to HiZ-state.

Forced-CCM Mode (FCCM)

The low noise, forced-CCM mode disables the zero-crossing comparator, which means PWM signal won't have HiZ-state anymore unless negative over current protection is toggled. This causes the inductor current to reverse at light loads as the PWM loop needs to maintain a duty ratio V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant.

Power-On Reset (POR) and UVLO

Power-on reset (POR) occurs when V_{IN} rises above to approximately 4.5V (maximum), the RT2702 will prepare the PWM for operation. Once the input voltage decreases by approximately 500mV, the VIN under voltage-lockout (UVLO) circuitry will disable the external driver by setting $\overline{DISB}$ low.

Enable and Disable

EN controls the power-up sequencing of the linear regulator (VDRV) and buck controller. The RT2702 remains in shutdown if the EN pin is lower than 0.8V. When EN pin rises above the 1.05V, the RT2702 will begin a new initialization and soft-start procedure.

Linear Regulator (VDRV)

The RT2702 contains a 5V (VDRV) linear regulator, which can afford at least 100mA loading. This regulator will be turned on only when V_{IN} rises above POR threshold 4.5V and EN is higher than 1.2V.

External Driver Enable ($\overline{DISB}$)

The RT2702 provides an output pin $\overline{DISB}$ to turn on/off external DrMOS. When the linear regulator VDRV soft-start is finished, $\overline{DISB}$ will be pulled high to 5V. Then the RT2702 begins the soft-start procedure. In addition, if UVP or OTP occurs, $\overline{DISB}$ will be pulled low to disable DrMOS until the protections are clean.

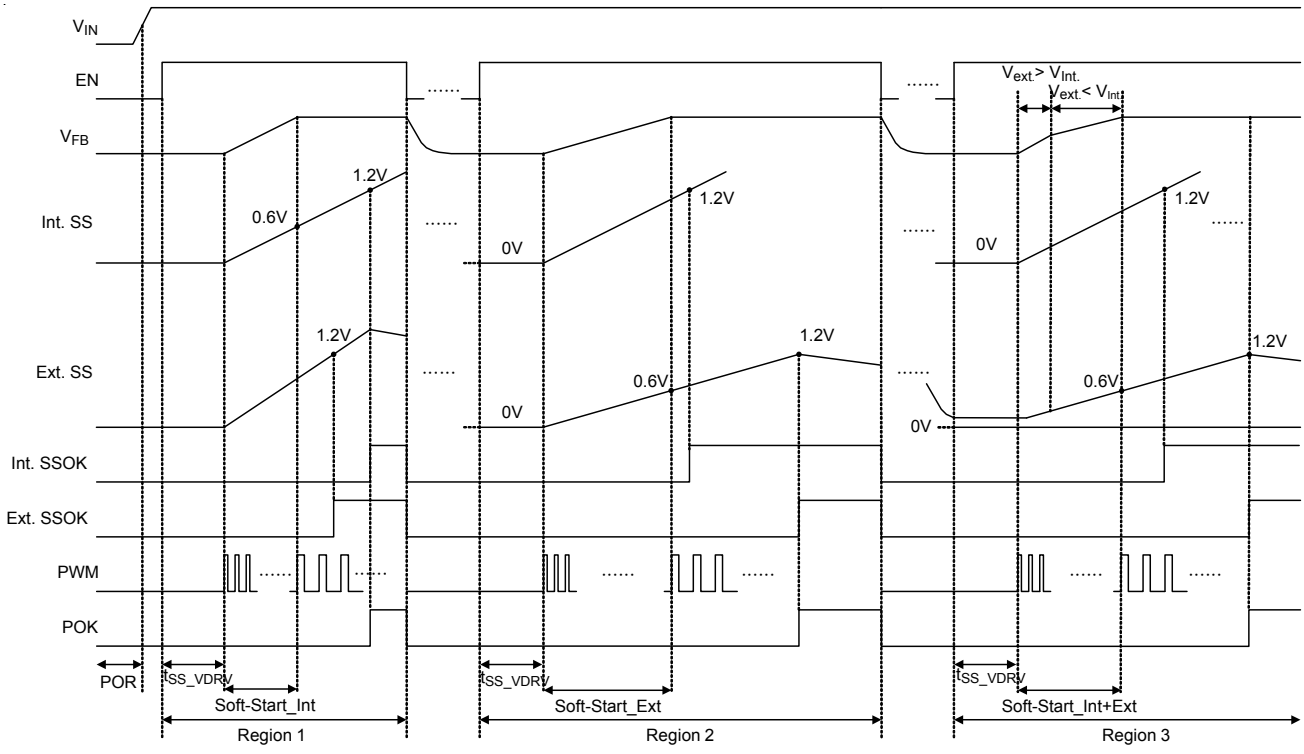


Figure 2. Soft-Start Sequence

Soft-Start

The RT2702 provides both internal soft-start function and external soft-start function. The soft-start function is implemented to prevent large inrush current and output voltage overshoot during the start-up procedure. The soft-start function automatically begins once the chip is enabled. V_{FB} will follow neither internal nor external soft-start voltage ramp, depends on which ramp has lower voltage. Since VDRV also has soft-start ramp, thus V_{FB} will begin ramping up after 3ms to 4ms from EN high.

As the region1 shown in the Figure 2, since external ramp is quicker and higher than internal ramp, thus V_{FB} follows internal ramp during soft-start procedure. V_{FB} will no longer follow internal ramp when it is close to V_{REF}, which is 0.6V, and sticks to the V_{REF}. The internal soft-start time is designed as a typical value 3ms from 10% to 90% V_{REF}. Soft-start procedure is finished after internal ramp rises above 1.2V, in the meantime, int. SSOK will be asserted high, and POK can be asserted high if OVP and UVP are not triggered.

As the region2 shown in the Figure 2, because external ramp is slower and lower than internal ramp, thus V_{FB} tracks external ramp during soft-start procedure. The behavior is similar to region1 except that soft-start time period is programmed. Note that SS pin would be left floating after both int. and ext. SSOK are asserted high to avoid SS pin having further disturbance to the loop. The function block diagram of SS pin is shown in Figure 3 below. The RT2702 starts sourcing 10μA toward C_{SS} which is connected to SS pin. SS pin would be discharged when system shuts down or re-starts up.

The external soft-start time can be calculated as :

$$t_{SS\_Ext.} = \frac{C_{SS} \times V_{REF}}{10\mu A}$$

Where V_{REF} is 0.6V, and C_{SS} is the external capacitor placed between SS pin and GND.

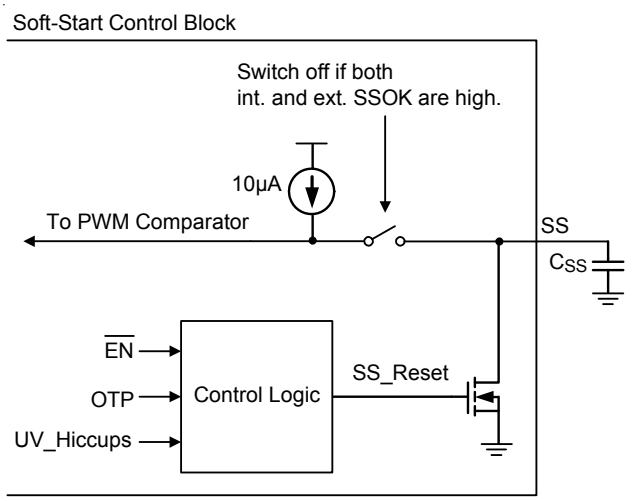


Figure 3. Soft-Start Control Block.

As the region3 shown in the Figure 2, if system is enabled with SS pin having residual voltage, then V_{FB} follows internal ramp in the beginning since the voltage of internal ramp is lower than external ramp($V_{Ext.} > V_{Int.}$). Afterwards, V_{FB} begins to track external ramp when the voltage of external ramp is lower than internal ramp($V_{Ext.} < V_{Int.}$).

POK

The POK pin is the output of an open-drain buffer, thus it requires a pull-up resistor. POK goes high when soft-start is finished and has no UVP nor OVP.

Current Limit

The RT2702 provides cycle-by-cycle current limit control by comparing the C_{SEN} voltage V_{CSEN} and R_{CS} voltage V_{CS} of DCR circuitry to determine the turn-on timing of PWM. The current limit circuit employs a unique "valley" current sensing algorithm as shown in Figure 4. If the magnitude of the C_{SEN} voltage signal of DCR circuitry is above the current limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds the average output inductor current. Eventually, output drops lower than the under-voltage protection threshold, inducing IC shutdown.

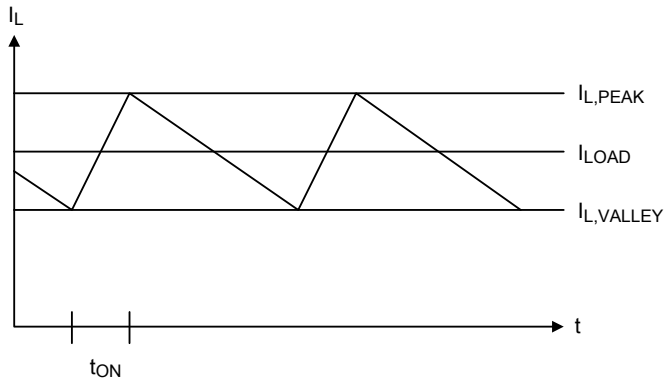


Figure 4. "Valley" Current Limit

Current Limit Threshold Setting

Current limit threshold can be set by two resistors, one is R_{ILIM} between ILIM and GND, and other is R_{CS} of the DCR circuit, as shown in Figure 5. Once V_{IN} exceeds the POR threshold and chip is enabled, an internal voltage source 1.2V will be generated, and then the current I_{ILIM} will flow through R_{ILIM}. In Figure 5, I_{ILIM} is mirrored to flow through R_{CS} of the DCR circuit by current mirror, and then the voltage V_{CS} will be generated. With the DCR circuit, the C_{SEN} voltage V_{CSEN} is inductor current I_L multiplied by inductor DCR $R_{L,DCR}$. By using an internal comparator in the RT2702, when V_{CSEN} valley is higher than the current limit protection threshold V_{CS}, the PWM is not allowed to initiate a new cycle.

Therefore, R_{ILIM} can be determined using the following equation :

$$R_{ILIM} = \frac{1.2 \times R_{CS}}{I_{L,VALLEY} \times R_{L,DCR}}$$

where $I_{L,VALLEY}$ represents the desired inductor limit current (valley inductor current).

Besides, in order to ensure the I_L waveform can be reflected on V_{CSEN}, the time constant setting should follow the equation below :

$$R_{SEN} \times C_{SEN} = \frac{L}{R_{L,DCR}}$$

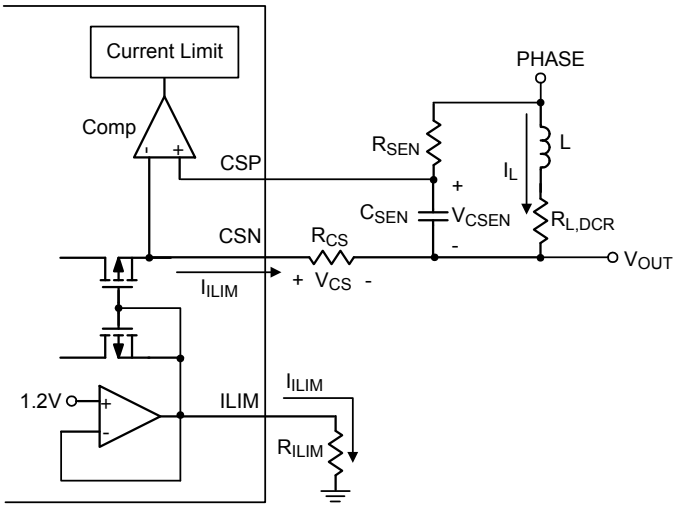


Figure 5. External Current Limit Setting

Thermal Compensation for Current Sense

Since the copper wire of inductor has a positive temperature coefficient. And hence, temperature compensation is necessary for the lossless inductor current sense. Figure 6 shows the thermal compensation method for current sense circuit that is not only simple but also effective way to compensate temperature variation. An NTC thermistor is employed in the thermal compensation network, and it can be used to compensate DCR variation when temperature is changed. Usually, R_P is set equal to R_{NTC}(25°C). R_S is selected to linearize the NTC's temperature characteristic. For a given R_{NTC}, R_{SEN} and R_S can be obtained to compensate the temperature variation of the sense resistor. Besides, the optional C_{BYPASS} is used to reduce noise to affect the current sense network.

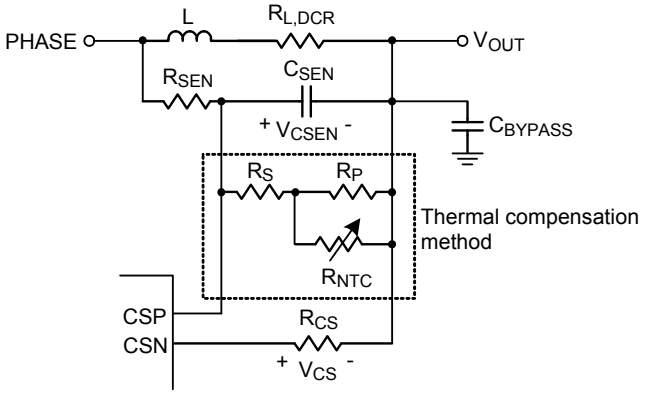


Figure 6. Thermal Compensation Method

Let

$$R_{EQU} = R_S + (R_P // R_{NTC})$$

According to current sense network and temperate, the corresponding equation is represented as follows :

$$\frac{L}{R_{L,DCR}} = C_{SEN} \times \frac{R_{EQU} \times R_{SEN}}{R_{EQU} + R_{SEN}}$$

Next, let

$$m = \frac{L}{R_{L,DCR} \times C_{SEN}}$$

Then

$$m \times \left(R_{SEN} + R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right) = R_{SEN} \times \left(R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right)$$

Step 1 : Given the two system temperature T_L and T_H at which are compensated.

Step 2 : Two equations can be listed as

$$m(T_L) \times \left(R_{SEN} + R_S + \frac{R_{NTC}(T_L) \times R_P}{R_{NTC}(T_L) + R_P} \right)$$
$$= R_{SEN} \times \left(R_S + \frac{R_{NTC}(T_L) \times R_P}{R_{NTC}(T_L) + R_P} \right)$$

$$m(T_H) \times \left(R_{SEN} + R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right)$$
$$= R_{SEN} \times \left(R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right)$$

Step 3 : Since R_P is usually set equal to R_{NTC}(25°C), two unknowns, R_{SEN} and R_S, can be calculated using two equations.

Output Over-Voltage Protection (OVP)

The voltage on the FB pin is monitored for over-voltage protection. When the FB voltage exceeds 12.5% of its set voltage threshold, over-voltage protection is triggered, then the signal of POK and PWM go low. This behavior should command DrMOS to discharge the output capacitor. A 10µs delay is applied to OVP detection circuit to prevent false trigger.

Besides, anti-overshoot(AOS) would be triggered when V_{FB} is above 642mV (V_{REF} + 42mV) and then PWM becomes tri-state. Thus more power, which is stored in inductor, would be eliminated by the body diode of LSMOS in DrMOS, and prevents V_{OUT} from having too much overshoot. If inductor has too much power stored in itself, then AOS won't be able to prevent system from triggering OVP. In this case, OVP would over-write AOS behavior, makes PWM go low and intends to discharge V_{OUT} with negative current on inductor.

Output Under-Voltage Protection (UVP)

The FB voltage is monitored for under voltage protection. When the FB voltage is less than 12.5% of its set voltage threshold during normal operation, under-voltage protection is triggered, then the signal of POK and $\overline{DISB}$ to be low. This behavior should turn off DrMOS. When UVP is triggered, the controller begins hiccup procedure and re-boost after 20ms. A 10µs delay is applied to UVP detection circuit to prevent false trigger.

Over-Thermal Protection (OTP)

The RT2702 features an over-thermal protection circuitry to prevent damage from excessive heat dissipation. The OTP function occurs when the die temperature exceeds 150°C, then $\overline{DISB}$ goes low and turns off internal linear regulator. Once the junction temperature is cooled down by approximately 25°C, the RT2702 will reboost from the beginning.

Thermal Shutdown Detection ($\overline{THWN}$)

The RT2702 has a thermal shutdown detection input $\overline{THWN}$ pin for external driver DrMOS. The RT2702 will pull low $\overline{DISB}$ if the voltage of thermal warning flag is lower than 0.4V.

Output Voltage Setting

The output voltage waveform is shown as Figure 7, which can be adjusted from 0.6V to 3.3V by setting the feedback resistors, R_{FB1} and R_{FB2} (see Figure 8). Choose R_{FB2} to be approximately 30k and solve for R_{FB1} using the equation below :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}} \right)$$

where the V_{REF} is 0.6V (typical), and the recommended output voltage range is between 0.6V and 3V.

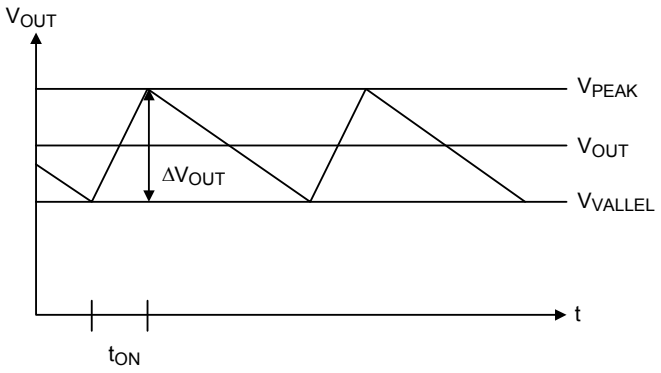


Figure 7. Output Voltage Waveform

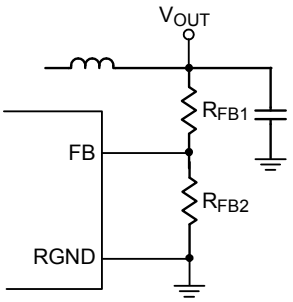


Figure 8. Setting with a Resistive Voltage Divider

Output Inductor Selection

Inductor plays an important role in step-down converters because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the dc resistance (DCR) of inductor should be as small as possible to minimize the copper loss. In addition, because inductor cost most of the board space, its size is also important. Low profile inductors can save board space especially when the height has limitation. However, low DCR and low profile inductors are usually cost ineffective. The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current, I_{PEAK}:

$$I_{PEAK} = I_{LOAD(MAX)} + \left[(LIR / 2) \times I_{LOAD(MAX)} \right]$$

This inductor ripple current also impacts transient-response performance, especially at low $V_{IN} - V_{OUT}$ differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient (V_{SAG}) is also a function of the output transient. V_{SAG} also features a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L(t_{ON} + t_{OFF\_MIN})}{2 \times C_{OUT} \times \left[V_{IN} \times t_{ON} - V_{OUT} \times (t_{ON} + t_{OFF\_MIN}) \right]}$$

where minimum off-time, t_{OFF_MIN}, is 275ns typically.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

where V_{P-P} is the peak-to-peak output voltage ripple.

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

The amount of overshoot due to stored inductor energy can be calculated as :

$$V_{SOAR} = \frac{(I_{PEAK})^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for a WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

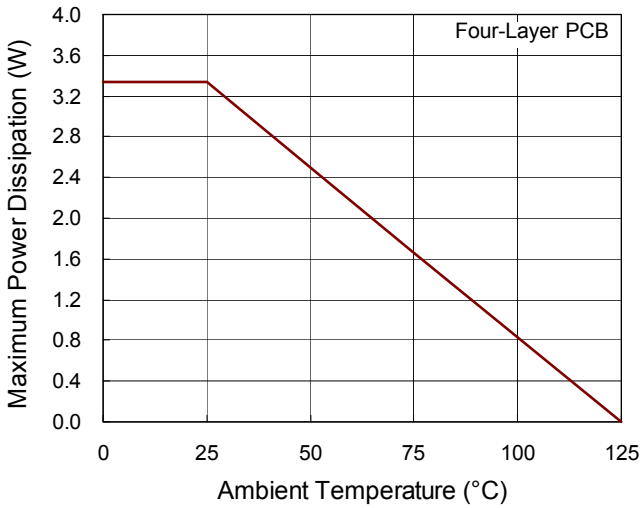


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to converter instability. Certain points must be considered before starting a layout for the RT2702.

- Connecting capacitors to VIN and VDRV are recommended. Place these capacitors close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the RT2702 to DrMOS should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as TON, EN, ILIM, SS, FB, CSN, CSP, POK, MODE, PWM, $\overline{DISB}$, $\overline{THWN}$, GND and RGND should be placed away from high voltage switching nodes such as PHASE nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Layout Guideline of Current Sense Circuit

An example of PCB layout guide is shown in Figure 10 for reference.

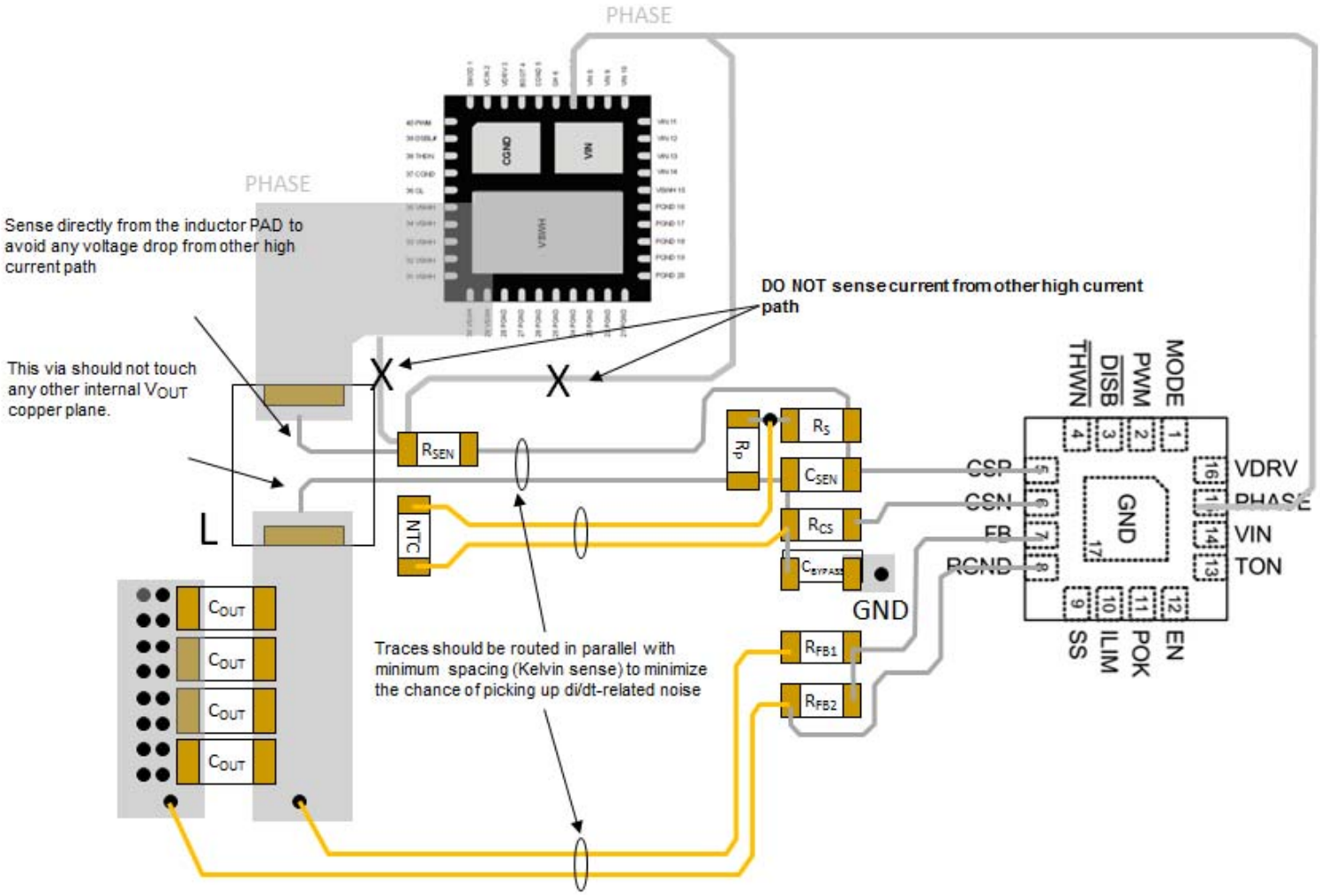
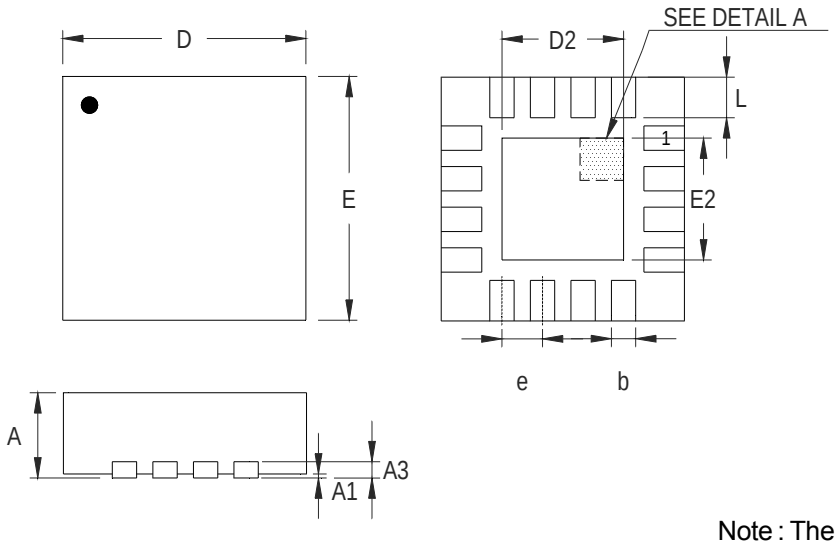
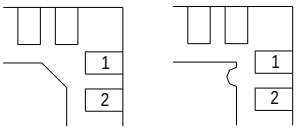


Figure 10. PCB Layout Guide

- In general, the small signal nets can be narrow and routed with 10 to 15 mil wide traces.
- The rule of thumb of the gap between is 1~2xtrace width.
- Clearance from other aggressor is 3xtrace width.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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