

MOSFET - Power, Single N-Channel, WDFN6 30 V, 4.9 - 18.9 mΩ, 17.2 A



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NTLJS3D9N03C

Features

- Small Footprint (4 mm²) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS Compliant

Applications

- Wireless Chargers
- Power Load Switch
- Power Management and Protection
- Battery Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V _{DSS}	30	V	
Gate-to-Source Voltage	V _{GS}	±12	V	
Continuous Drain Current R _{θJA} (Notes 1, 3)	Steady State	T _A = 25°C	I _D 17.2	A
		T _A = 85°C	12.4	
		T _A = 25°C	P _D 2.40	W
Continuous Drain Current R _{θJA} (Notes 2, 3)	Steady State	T _A = 25°C	I _D 10.3	A
		T _A = 85°C	7.4	
		T _A = 25°C	P _D 0.86	W
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs	I _{DM} 71	A	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

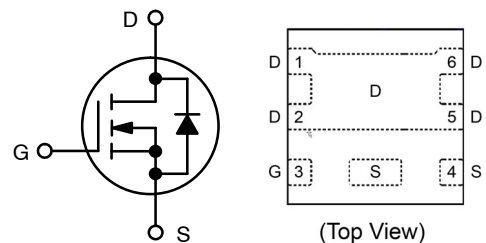
THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	R _{θJA}	52	°C/W
Junction-to-Ambient - Steady State (Note 2)	R _{θJA}	145	

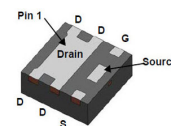
1. Surface-mounted on FR4 board using 1 in² pad size, 2 oz. Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. R_{θCA} is determined by the user's board design.

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
30 V	4.9 mΩ @ 4.5 V	17.2 A
	6.8 mΩ @ 3.3 V	
	10 mΩ @ 2.5 V	
	18.9 mΩ @ 1.8 V	

ELECTRICAL CONNECTION



N-CHANNEL MOSFET



WDFN6 (2.05x2.05)
CASE 483AV

MARKING DIAGRAM

YWZZ
A3D9
○

YW = Date Code
ZZ = Assembly Lot Code
A = Assembly Site Code
A3D9 = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		24.5		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	0.6		1.1	V
Threshold Temperature Coefficient	V_{GS}/T_J	$I_D = 250\ \mu\text{A}$, ref to 25°C		-3.83		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		3.6	4.9	$\text{m}\Omega$
		$V_{GS} = 3.3\text{ V}, I_D = 5\text{ A}$		4.1	6.8	
		$V_{GS} = 2.5\text{ V}, I_D = 4\text{ A}$		5.4	10	
		$V_{GS} = 1.8\text{ V}, I_D = 2\text{ A}$		9.8	18.9	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		69		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.65		Ω

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1.0\text{ MHz}$		1565		pF
Output Capacitance	C_{oss}			677		
Reverse Transfer Capacitance	C_{rss}			54.8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		14.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.17		
Gate-to-Source Charge	Q_{GS}			2.31		
Gate-to-Drain Charge	Q_{GD}			3.29		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 15\text{ V}, I_D = 10\text{ A}, R_G = 6\ \Omega$		10.1		ns
Rise Time	t_r			9.5		
Turn-Off Delay Time	$t_{d(off)}$			40.6		
Fall Time	t_f			15.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.75	1.2	V
			$T_J = 125^\circ\text{C}$		0.611		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 10\text{ A}$			31.7		ns
Reverse Recovery Charge	Q_{RR}				11.2		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

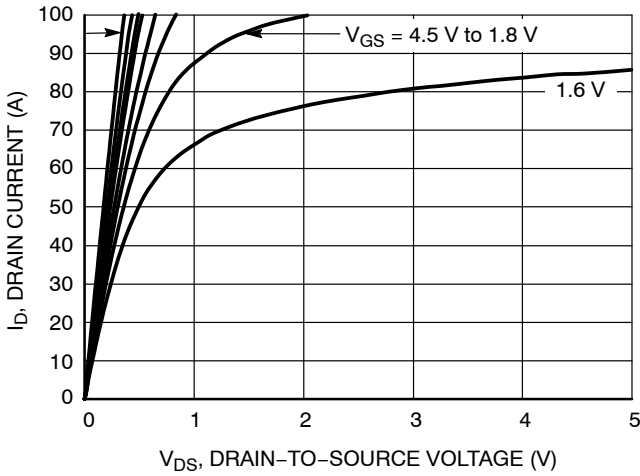


Figure 1. On-Region Characteristics

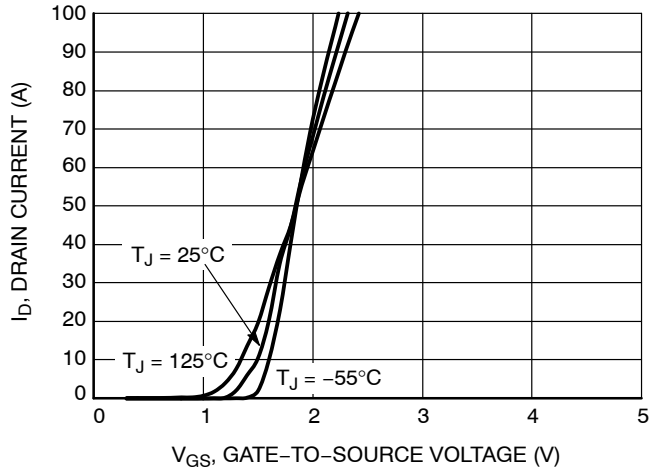


Figure 2. Transfer Characteristics

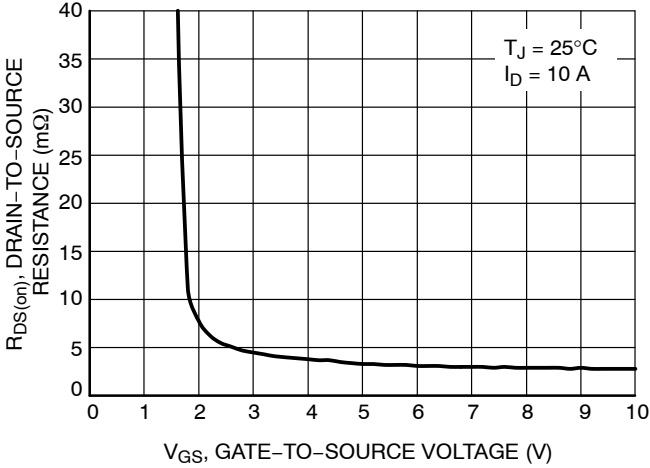


Figure 3. On-Resistance vs. Gate-to-Source Voltage (V)

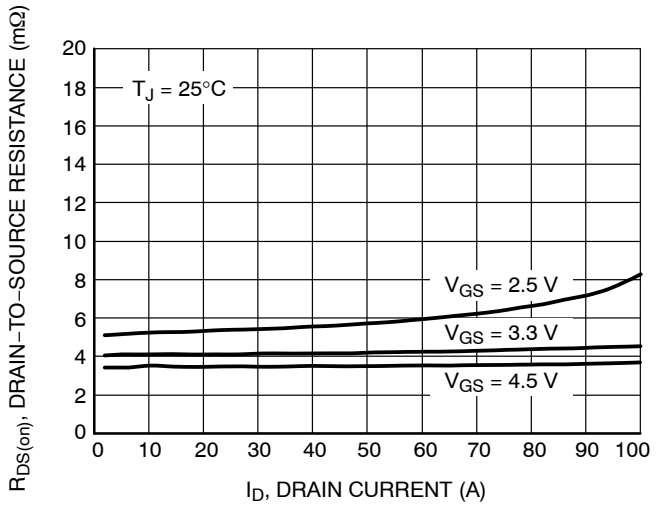


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

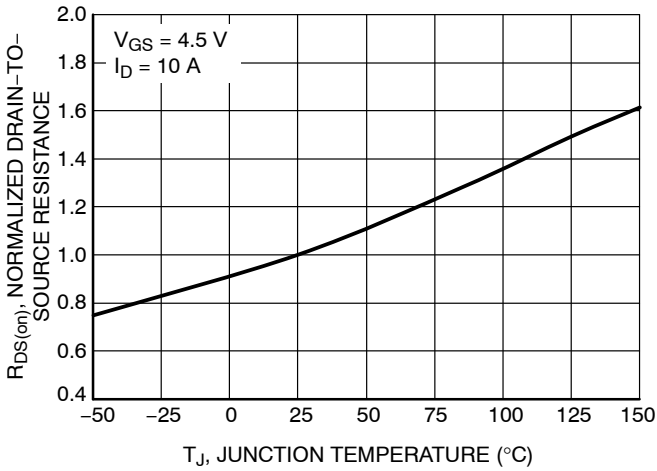


Figure 5. On-Resistance Variation with Temperature

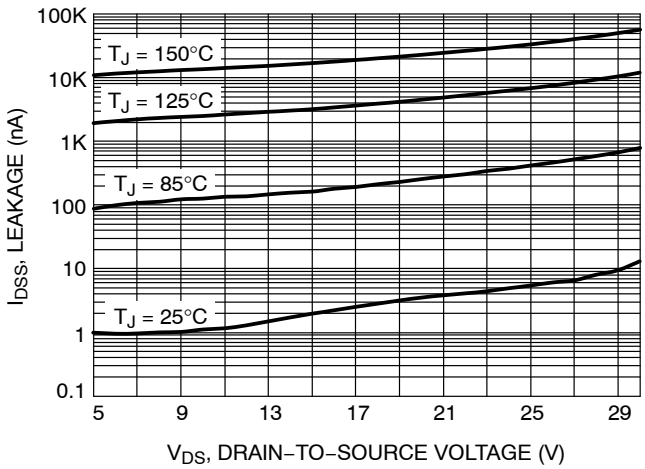


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

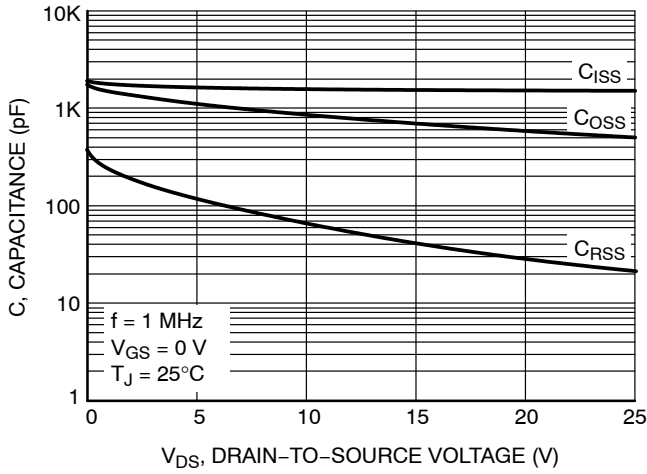


Figure 7. Capacitance Variation

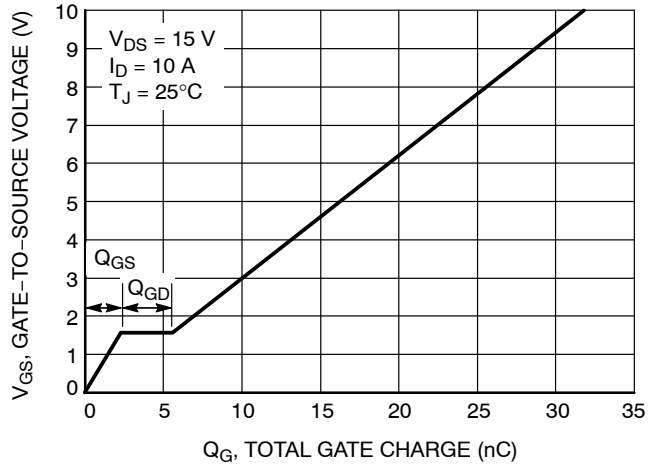


Figure 8. Gate-to-Source vs. Total Charge

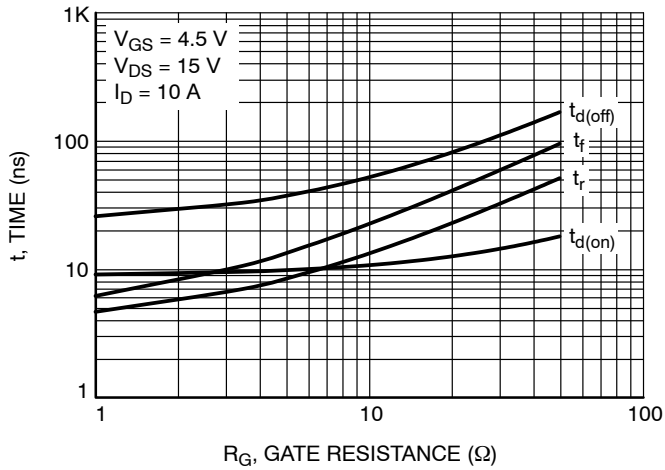


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

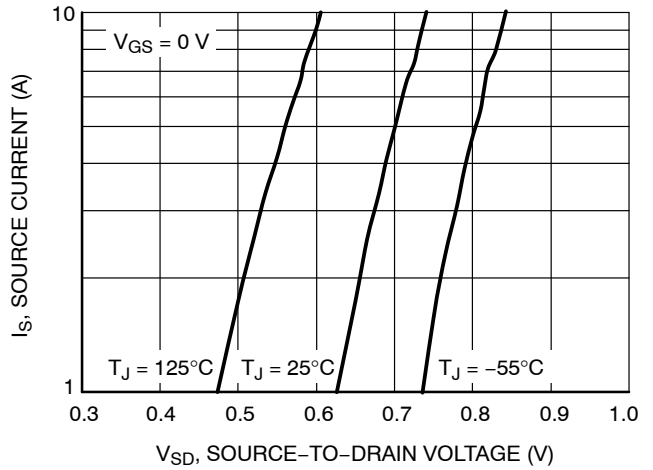


Figure 10. Diode Forward Voltage vs. Current

DEVICE ORDERING INFORMATION

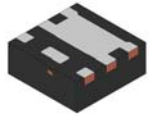
Device	Package	Shipping†
NTLJS3D9N03CTAG	WDFN6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

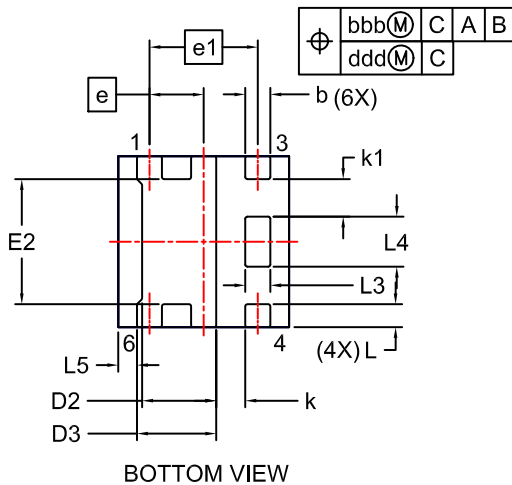
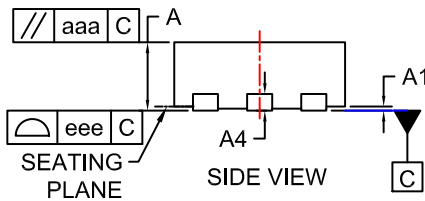
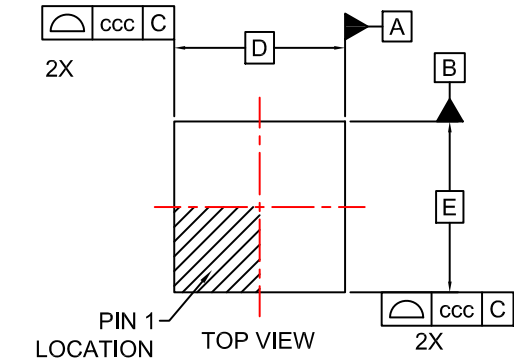
PACKAGE DIMENSIONS

ON Semiconductor®

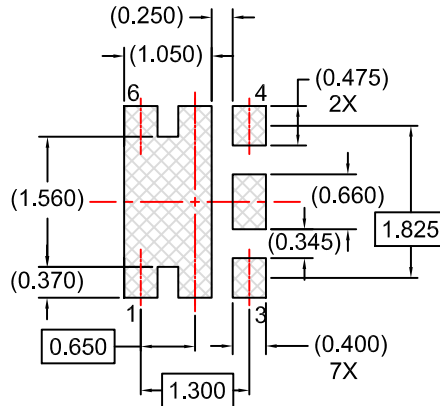


WDFN6 2.05X2.05, 0.65P
CASE 483AV
ISSUE A

DATE 02 APR 2019



LAND PATTERN RECOMMENDATION



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.00	-	0.05
A4	(0.20)		
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
D3	(0.95)		
E	1.95	2.05	2.15
E2	1.45	1.50	1.55
e	0.65 BSC		
e1	1.30 BSC		
k	(0.35)		
k1	(0.45)		
L	0.18	0.28	0.38
L3	0.25	0.30	0.35
L4	0.55	0.60	0.65
L5	(0.23)		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		
eee	0.05		

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