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Devices Connected/Referenced	
AD5542A/ AD5541A	16-Bit Voltage Output *nano*DAC® with 1 µs Settling Time
ADR421	2.5 V XFET® Low Noise, Precision Voltage Reference
AD8675	Precision Operational Amplifier
OP1177	Precision Operational Amplifier

How to Achieve High Precision Voltage Level Setting Using the AD5542A/AD5541A 16-Bit Voltage Output DAC

## CIRCUIT FUNCTION AND BENEFITS

Achieving true 16-bit performance with a voltage output DAC requires selecting not only the correct DAC but also the correct complementary supporting components. This circuit provides a low risk solution for precision 16-bit digital-to-analog conversion using the AD5542A/AD5541A voltage output DAC with the ADR421 voltage reference and the AD8675 ultralow offset op amp used as the voltage reference buffer.

The reference buffer is critical to the design because the input impedance at the DAC reference input is heavily code- dependent and will lead to linearity errors if the DAC reference is not adequately buffered. With a high open-loop gain of 120 dB, the AD8675 has been proven and tested to meet the settling time, offset voltage, and low impedance drive capability required by this circuit application.

The precision, low offset OP1177 can be used as an optional output buffer if needed.

This combination of parts provides industry-leading 16-bit integral nonlinearity (INL) of ±1 LSB and differential nonlinearity (DNL) of ±1 LSB with guaranteed monotonicity, as well as low power, small PCB area, and cost effectiveness.
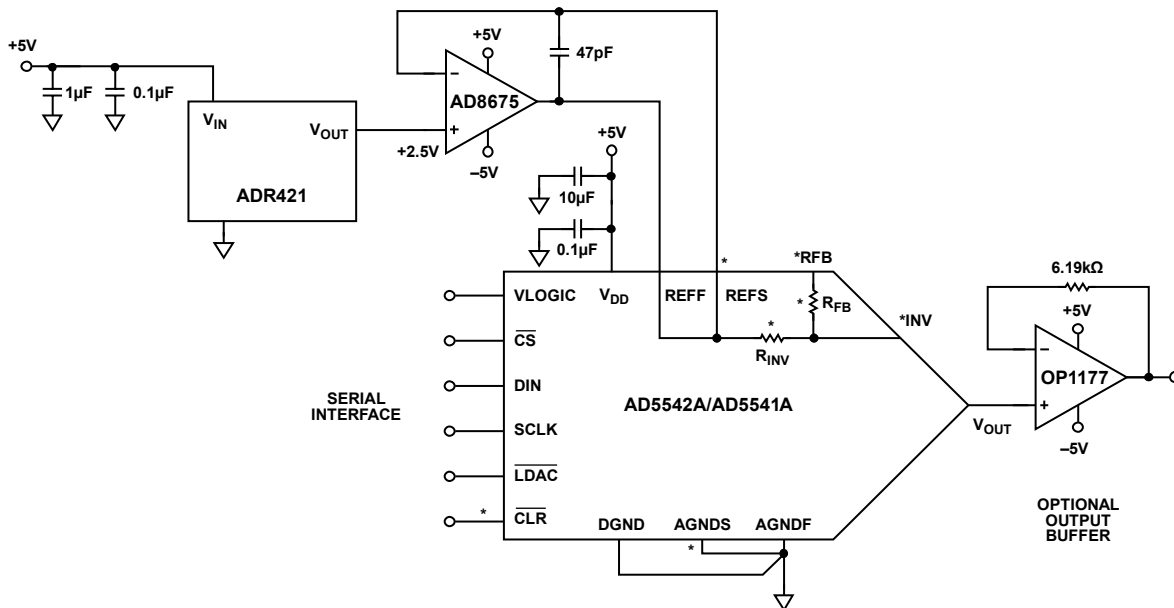
* FUNCTION AVAILABLE ON AD5542A.

Figure 1. Precision DAC Configuration (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

For a perfect DAC with no errors, output voltage is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where D is the decimal data word loaded in the DAC register, and N is the resolution of the DAC.

For a reference of 2.5 V, and N = 16, the equation simplifies to the following:

$$V_{OUT} = \frac{2.5 \times D}{65,536}$$

This gives a V_{OUT} of 1.25 V at mid-scale, and 2.5 V at full-scale.

The LSB size is 2.5 V/65,536 = 38.1 μV.

One LSB at 16 bits is also 0.0015% of full-scale or 15 ppm FS.

The initial room temperature accuracy of the ADR421 (B-grade) reference is 0.04%, which is approximately 27 LSBs at 16 bits. This initial error can be removed with a system calibration. The temperature coefficient of the ADR421 (B-grade) is 1 ppm/°C typical, 3 ppm/°C maximum.

Assuming a perfect reference (the reference error removed by system calibration), the worst-case unipolar output voltage (including errors) for the AD5542A can be calculated from the following equation:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL$$

where:

$V_{OUT-UNI}$ is unipolar mode worst-case output.

D is code loaded to the DAC.

V_{REF} is reference voltage applied to the DAC (assumed to have no errors).

V_{GE} is gain error in volts. (Note that the offset error of the reference buffer must be included in the gain error, hence the op amp chosen for the reference buffer must have low input offset voltage).

V_{ZSE} is zero-scale error (offset error) in volts. (Note that the offset voltage of the optional output buffer amplifier would add to this error)

INL is integral nonlinearity of the DAC in volts. (Note that the nonlinearity of the optional output buffer amplifier would add to this error).

The zero-scale error and gain error of this circuit were measured to be ±0.7 LBSs and ±2 LSBs, respectively, at ambient temperature. Over temperature (−40°C to +85°C) the zero-scale error is ±1.5 LSBs, and the gain error ±3 LSBs. These measurements were taken directly from the V_{OUT} of the AD5542A without an output buffer connected.

This circuit utilizes the AD5542A voltage output DAC, providing true 16-bit INL and DNL. The DAC architecture of the AD5541A/AD5542A is a segmented R-2R voltage mode DAC. With this type of configuration, the output impedance is independent of code, but the input impedance seen by the reference is heavily code dependent. For this reason, the reference buffer choice is very important to account for code-dependent reference current, which may lead to linearity errors if the DAC reference is not adequately buffered. The op amp open-loop gain, offset voltage, offset error temperature coefficient, and voltage noise are also important selection criteria when selecting a reference buffer with precision voltage output DACs. Offset errors in the reference circuit result in gain error on the DAC output.

This circuit employs an AD8675 op amp in a force and sense configuration (Kelvin sensing) as the low impedance output reference buffer for the AD5542A. The AD8675 has an open-loop gain of 120 dB and is a precision, 36 V, 2.8 nV/√Hz op amp. With a typical offset voltage of 10 μV, typical drift of less than 0.2 μV/°C, and noise of 0.1 μV p-p (0 Hz to 10 Hz), the AD8675 is well suited for applications where error sources need to be minimized.

The AD5542A can be operated in either buffered or unbuffered mode. The application and its requirements on settling time, load impedance, noise, etc., determine which mode of operation to be used. The output buffer can be chosen to optimize dc precision or fast settling time. The optional output amplifier in this circuit is the high precision OP1177. Output impedance of the DAC is constant (typically 6.25 kΩ) and code-independent, but to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The output amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The output amplifier adds another time constant to the system, hence increasing the settling time of the output. A wider bandwidth op amp results in a shorter effective settling time of the combined DAC and amplifier.

The combination of parts shown in Figure 1 minimizes PC board area. The AD5542A is available in a 3 mm × 3 mm 16-lead LFCSP or 16-lead TSSOP package. The AD5541A is available in 3 mm × 3 mm, 10-lead LFCSP or 10-lead MSOP.

Note that the AD5541A does not contain the Kelvin sense lines on the reference and the ground, the Clear function, or the R_{FB} and R_{INV} resistors.

The AD8675 and ADR421 are available in an 8-lead MSOP or SOIC , and the OP1177 is available in an 8-lead MSOP.

The optional output op amp is the OP1177 in a unity gain configuration, which includes a 6.19 kΩ resistor in series with the inverting input. This resistor is used for bias current cancellation and matches the output resistance of the AD5542A, which is approximately 6.25 kΩ ± 20%.

Measured results show that the AD5542A/AD5541A is an excellent candidate for high accuracy, low noise performance
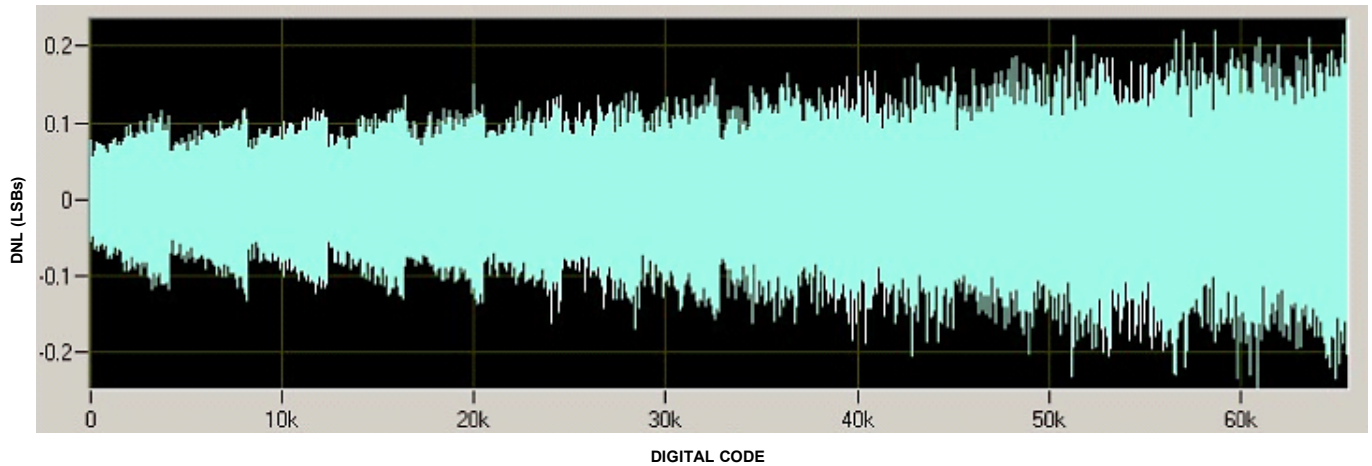
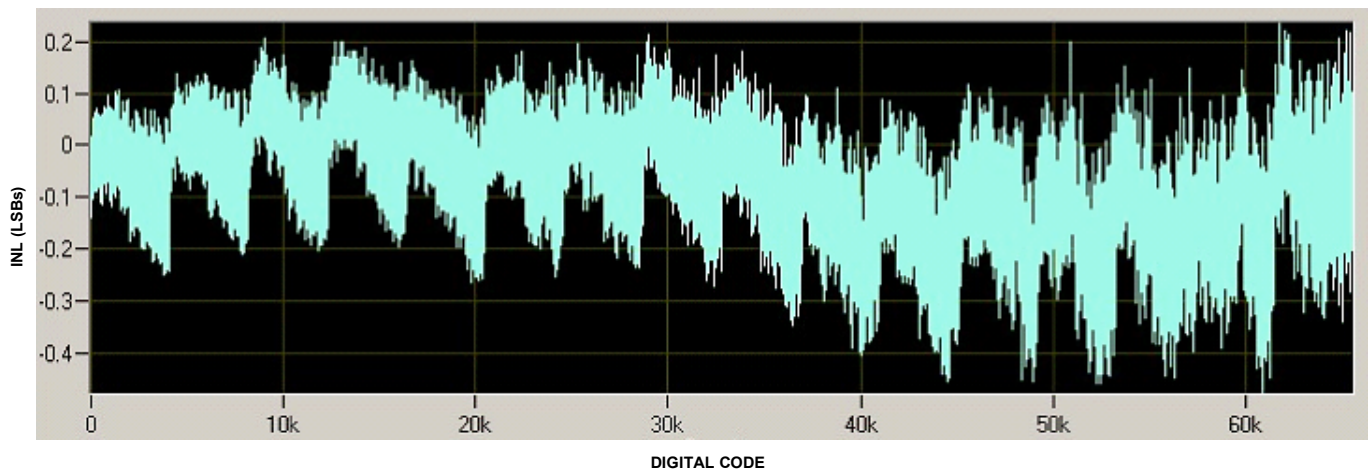Figure 2. Differential Nonlinearity

Figure 3. Integral Nonlinearity

level setting applications. The level of dc performance is maintained using the ADR421 reference and the AD8675 as a reference buffer in this high accuracy, high performance system. The measurements were made directly at V_OUT without the optional output buffer connected.

Integral Nonlinearity and Differential Nonlinearity Measurements

INL error is the deviation in LSB of the actual DAC transfer function from an idealized transfer function. DNL error is the difference between an actual step size and the ideal value of 1 LSB. The circuit in Figure 1 provides 16-bit resolution with ±1 LSB DNL and INL. Figure 2 and Figure 3 show the DNL and INL performance of the circuit.

Zero-Code and Gain Error Measurements

The zero-scale error (V_{ZSE}) and gain error (V_{GE}) were measured to be ±0.7 LBSs and ±2 LSBs, respectively, at ambient temperature. Over temperature (−40°C to +85°C) the zero-scale error is ±1.5 LSBs, and the gain error ±3 LSBs.

Layout Considerations

In any circuit where accuracy is important, it is important to consider the power supply and ground return layout on the board. The printed circuit board (PCB) containing the circuit should have separate analog and digital sections. If the circuit is used in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5542A/AD5541A. The circuit should be constructed on a multilayer PCB with a large area ground plane layer and a power plane layer. See the MT-031 Tutorial for more discussion on layout and grounding.

The power supply to the AD5542A/AD5541A should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be as physically close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitor should be either the tantalum bead type or ceramic type. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and low effective series inductance (ESL), such as is typical of common ceramic types of capacitors.

This 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching. See the MT-101 Tutorial for more details on proper decoupling techniques.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground.

COMMON VARIATIONS

The AD8628 is another excellent op amp for use as the reference buffer in this circuit. It provides a low offset voltage and ultra low bias current with an open-loop gain of 125 dB. The ADR421 (2.5 V) can be replaced by either the ADR423 (3.00 V) or ADR424 (4.096 V), which are low noise references available from the same reference family as the ADR421. The ADR441 and ADR431 ultralow noise references are also suitable substitutes, which provide 2.5 V.

The AD8661 is a good alternate choice for the optional output buffer. This is a CMOS op amp that uses the ADI patented DigiTrim® technique to achieve low offset voltage. It features low input bias current and wide signal bandwidth.

The AD8605 or AD8655 (both are single supply, +2.7 V to +5.5 V) would also be options, but their outputs will have nonlinearity near zero-volts output because of the output stage limitations of all rail-to-rail op amps (see the MT-035 Tutorial).

The AD5542A contains internal resistors (R_{FB} and R_{INV}), which can be used with an external op amp to provide a bipolar voltage output. (See the AD5542A data sheet for further details).

LEARN MORE

Kester, Walt. 2005. *The Data Conversion Handbook.* Analog Devices. Chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs.* Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs,* Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND.* Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues,* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

Voltage Reference Wizard Design Tool.

Data Sheets and Evaluation Boards

AD5542A Data Sheet

AD5541A Data Sheet

AD5542A Evaluation Board

AD5541A Evaluation Board

ADR421 Data Sheet

AD8675 Data Sheet

OP1177 Data Sheet

REVISION HISTORY

7/10—Revision 0: Initial Version

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