# Micropower, 3-Axis, ±200 *g* Digital Output, MEMS Accelerometer

## FEATURES

- ±200 *g* measurement range
- 160 Hz to 2560 Hz user selectable bandwidth with four-pole antialiasing filter
- Selectable oversampling ratio
- Adjustable high-pass filter
- Ultra low power
  - Power can be derived from a coin cell battery
  - 28 µA at 2560 Hz ODR, 3.3 V supply
  - Low power, wake-up mode for low *g* activity detection
  - 1.7 µA instant on mode with adjustable threshold
  - <0.1 µA standby mode
- Built in features for system level power savings
- Deep embedded FIFO to minimize host processor load
  - Autonomous interrupt processing without processor intervention
- Ultra low power event monitoring detects impacts and wakes up fast enough to capture the transient events
- Adjustable, low *g* threshold activity and inactivity detection
- Wide operating voltage range: 2.5 V to 3.5 V
- Acceleration sample synchronization via external trigger
- SPI digital interface and I2C interface format support
- 12-bit output at 100 m*g*/LSB scale factor
- Wide temperature range: −40°C to +105°C
- Small, thin, 3 mm × 3.25 mm × 1.06 mm package

## APPLICATIONS

- Impact and shock detection
- Asset health assessment
- Portable Internet of Things (IoT) edge nodes
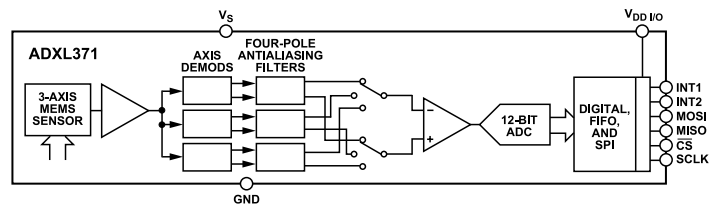- Concussion and head trauma detection

## FUNCTIONAL BLOCK DIAGRAM

## GENERAL DESCRIPTION

The ADXL371 is an ultra low power, 3-axis, ±200 *g* microelectromechanical system (MEMS) accelerometer that consumes 28 µA at a 2560 Hz output data rate (ODR). The ADXL371 does not power cycle its front end to achieve its low power operation and therefore does not run the risk of aliasing the output of the sensor.

In addition to its ultra low power consumption, the ADXL371 enables impact detection while providing system level power reduction. The device includes a deep multimode output first in, first out (FIFO), several activity detection modes, and a method for capturing only the peak acceleration of overthreshold events.

Two additional lower power modes with interrupt driven, wake-up features are available for monitoring motion during periods of inactivity. In wake-up mode, acceleration data can be averaged to obtain a low enough output noise to trigger on low *g* thresholds. In instant on mode, the ADXL371 consumes 1.7 µA while continuously monitoring the environment for impacts. When an impact event that exceeds the internally set threshold is detected, the device switches to normal operating mode fast enough to record the event.

High *g* applications tend to experience acceleration content over a wide range of frequencies. The ADXL371 includes a four-pole, low-pass antialiasing filter to attenuate out of band signals that are common in high *g* applications. The ADXL371 also incorporates a high-pass filter to eliminate initial and slow changing errors, such as ambient temperature drift.

The ADXL371 provides 12-bit output data at a 100 m*g*/LSB scale factor. The user can access configuration and data registers via the serial peripheral interface (SPI) or I2C protocol. The ADXL371 operates over a wide supply voltage range and is available in a 3 mm × 3.25 mm × 1.06 mm package.

In this data sheet, multifunction pin names may be referenced by their relevant function only.



*Figure 1.*

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## REVISION HISTORY

**10/2022—Rev. 0 to Rev. A**

**3/2021—Revision 0: Initial Version**

## SPECIFICATIONS

$T_A$ = 25°C, $V_S$ = 3.3 V, $V_{DDI/O}$ = 3.3 V, 2560 Hz ODR, 1280 Hz bandwidth, acceleration = 0 $g$, and default register settings but with high-pass filter (HPF) turned off. All minimum and maximum specifications are guaranteed. Typical specifications may not be guaranteed.

*Table 1.*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SENSOR INPUT | Each axis | | | | |
| Measurement Range | | | ±200 | | $g$ |
| Nonlinearity | Percentage of full scale | | ±0.5 | | % |
| Sensor Resonant Frequency | | | 16 | | kHz |
| Cross Axis Sensitivity[1] | | | ±2.5 | | % |
| OUTPUT RESOLUTION | Each axis | | | | |
| All Operating Modes | | | 12 | | Bits |
| SCALE FACTOR | Each axis | | | | |
| Scale Factor Calibration Error | | | | ±10 | % |
| Scale Factor at $X_{OUT}$, $Y_{OUT}$, $Z_{OUT}$ | Expressed in m$g$/LSB | | 100 | | m$g$/LSB |
| | Expressed in LSB/$g$ | | 10 | | LSB/$g$ |
| Scale Factor Change Due to Temperature[2] | | | 0.1 | | %/°C |
| 0 $g$ OFFSET | Each axis | | | | |
| 0 $g$ Output | $X_{OUT}$, $Y_{OUT}$, and $Z_{OUT}$, and at 5120 Hz ODR, 2560 Hz bandwidth | | | | |
| | $V_S$ = 3.3 V | −3 | ±1 | +3 | $g$ |
| | 2.5 V ≤ $V_S$ ≤ 3.5 V | −8 | ±1 | +8 | $g$ |
| 0 $g$ Offset vs. Temperature[2] | $X_{OUT}$, $Y_{OUT}$, $Z_{OUT}$ | | ±30 | | m$g$/°C |
| NOISE PERFORMANCE | | | | | |
| Noise Bandwidth | Each axis | | | | |
| Normal Operation | | | 6.5 | | m$g$/√Hz |
| Low Noise Mode | | | 5.5 | | m$g$/√Hz |
| BANDWIDTH | User selectable | | | | |
| ODR | | 320 | | 5120 | Hz |
| High-Pass Filter, −3 dB Corner[3] | | 0.19 | | 24.38 | Hz |
| Low-Pass (Antialiasing) Filter, −3 dB Corner[4] | Four-pole low-pass filter | 160 | | 2560 | Hz |
| POWER SUPPLY | | | | | |
| Operating Voltage Range ($V_S$) | | 2.5 | 3.3 | 3.5 | V |
| Input and Output Voltage Range ($V_{DDI/O}$)[5, 6] | | 2.5 | 3.3 | $V_S$ + 0.3 | V |
| Supply Current | | | | | |
| Measurement Mode | 2560 Hz ODR | | | | |
| Normal Operation | | | 28 | | µA |
| Low Noise Mode | | | 37 | | µA |
| Instant On Mode | | | 1.7 | | µA |
| Wake-Up Mode | Varies with wake-up rate | | | | |
| | At slowest wake-up rate | | 1 | | µA |
| Standby Mode | | | <0.1 | | µA |
| Power Supply Rejection Ratio (PSRR) | Source capacitance ($C_S$) = 1.1 µF, input and output capacitance ($C_{IO}$) = 1.1 µF, and input is 100 mV sine wave on $V_S$ | | | | |
| Input Frequency | | | | | |
| 100 Hz to 1 kHz | | | −20 | | dB |
| 1 kHz to 250 kHz | | | −17 | | dB |
| Turn-On Time | 2560 Hz ODR | | | | |
| Power-Up to Standby | $C_S$ = 1.1 µF and $C_{IO}$ = 1.1 µF | | 6.25 | | ms |
| Measurement Mode Instruction to First Data Output[7] | Filter settle bit = 1 | | 1 | | ms |

## SPECIFICATIONS

*Table 1.*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | Filter settle bit = 0 | | 462.5 | | ms |
| Instant On Ultra Low Power (ULP) Monitoring to Full Bandwidth Data | | | 1.25 | | ms |
| ENVIRONMENTAL TEMPERATURE | | | | | |
| Operating Temperature Range | | −40 | | +105 | °C |

[1]  Cross axis sensitivity is defined as coupling between any two axes.

[2]  The scale factor may change 0.1%/°C (typical) in the −40°C to +25°C or +25°C to +105°C temperature ranges.

[3]  This parameter has an available corner frequency scale with the ODR setting.

[4]  Bandwidth and ODR are set independent of each other.

[5]  This value is limited to 3.6 V, maximum.

[6]  The operating voltage range to all other pins (digital input/outputs (I/Os)) is limited to the absolute maximum ratings (see Table 4).

[7]  Data output before the 5th sample may be invalid due to filter settling.

## SPI SPECIFICATIONS

$T_A$ = 25°C, $V_S$ = 3.3 V, and $V_{DDI/O}$ = 3.3 V, unless otherwise noted.

*Table 2. SPI Logic Levels and Timing*

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| INPUT DC LEVELS | | | | | |
| $V_{IL}$ | Low level input voltage | | | 0.3 × $V_{DDI/O}$ | V |
| $V_{IH}$ | High level input voltage | 0.7 × $V_{DDI/O}$ | | | V |
| $I_{IL}$ | Low level input current, $V_{IN}$ = 0 V | −0.1 | | | µA |
| $I_{IH}$ | High level input current, $V_{IN}$ = $V_{DDI/O}$ | | | 0.1 | µA |
| OUTPUT DC LEVELS | | | | | |
| $V_{OL}$ | Low level output voltage, $I_{OL}$ = $I_{OL, MIN}$ | | | 0.2 × $V_{DDI/O}$ | V |
| $V_{OH}$ | High level output voltage, $I_{OL}$ = $I_{OH, MAX}$ | 0.8 × $V_{DDI/O}$ | | | V |
| $I_{OL}$ | Low level output current, $V_{OL}$ = $V_{OL, MAX}$ | −10 | | | mA |
| $I_{OH}$ | High level output current, $V_{OL}$ = $V_{OH, MIN}$ | | | 4 | mA |
| INPUT AC | | | | | |
| SCLK Frequency | | 0.1 | | 10 | MHz |
| $t_{HIGH}$ | SCLK high time | 40 | | | ns |
| $t_{LOW}$ | SCLK low time | 40 | | | ns |
| $t_{CSS}$ | $\overline{CS}$ setup time | 20 | | | ns |
| $t_{CSH}$ | $\overline{CS}$ hold time | 20 | | | ns |
| $t_{CSD}$ | $\overline{CS}$ disable time | 40 | | | ns |
| $t_{SCLKS}$ | Rising SCLK setup time | 20 | | | ns |
| $t_{SU}$ | MOSI setup time | 20 | | | ns |
| $t_{HD}$ | MOSI hold time | 20 | | | ns |
| OUTPUT AC | | | | | |
| $t_P$ | Propagation delay, $C_{LOAD}$ = 30 pF | | | 30 | ns |
| $t_{EN}$ | Enable MISO time | 30 | | | ns |
| $t_{DIS}$ | Disable MISO time | | | 20 | ns |

## SPECIFICATIONS

### SPI Timing Diagrams



*Figure 2. SPI Timing Diagram*



*Figure 3. SPI Timing Diagram, Single-Byte Read*
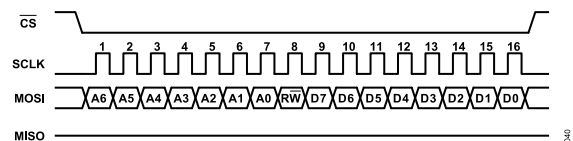


*Figure 4. SPI Timing Diagram, Single-Byte Write*
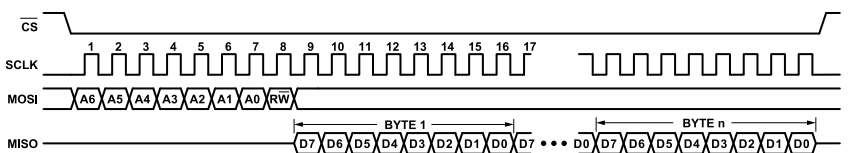


*Figure 5. SPI Timing Diagram, Multibyte Read*
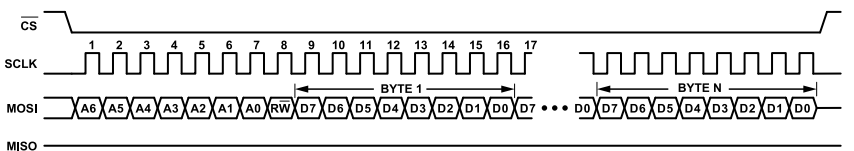


*Figure 6. SPI Timing Diagram, Multibyte Write*

## I$^2$C SPECIFICATIONS

$T_A$ = 25°C, $V_S$ = 3.3 V, $V_{DDI/O}$ = 3.3 V, unless otherwise noted.

*Table 3. I$^2$C Logic Level and Timing*

| Parameter | Description | I2C_HSM_EN = 0 | | | I2C_HSM_EN = 1 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| INPUT AC | | | | | | | | |
| SCLK Frequency | | 0 | | 1 | 0 | | 3.4 | MHz |
| $t_{HIGH}$ | SCLK high time | 260 | | | 120 | | | ns |
| $t_{LOW}$ | SCLK low time | 500 | | | 320 | | | ns |

## SPECIFICATIONS

*Table 3. I²C Logic Level and Timing*

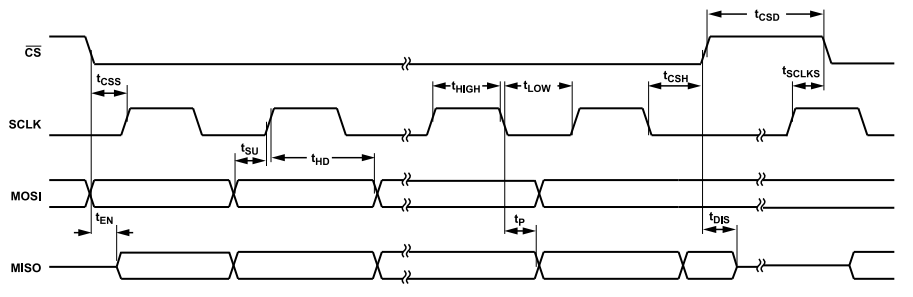| Parameter | Description | I2C_HSM_EN = 0 | | | I2C_HSM_EN = 1 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{SUSTA}$ | Start setup time | 260 | | | 160 | | | ns |
| $t_{HDSTA}$ | Start hold time | 260 | | | 160 | | | ns |
| $t_{SUDAT}$ | Data setup time | 50 | | | 10 | | | ns |
| $t_{HDDAT}$ | Data hold time | 0 | | | 0 | | 150 | ns |
| $t_{SUSTO}$ | Stop setup time | 260 | | | 160 | | | ns |
| $t_{BUF}$ | Bus free time | 500 | | | | | | ns |
| $t_{RCL}$ | SCL input rise time | | | 120 | 20 | | 80 | ns |
| $t_{FCL}$ | SCL input fall time | $20 \times (V_{DD}/5.5)$ | | 120 | 20 | | 80 | ns |
| $t_{RDA}$ | SDA input rise time | | | 120 | 20 | | 160 | ns |
| $t_{FDA}$ | SDA input fall time | $20 \times (V_{DD}/5.5)$ | | 120 | 20 | | 160 | ns |
| OUTPUT AC | | | | | | | | |
| $C_{LOAD}$ | | | | 550 | | | 400 | pF |

## I²C Timing Diagrams
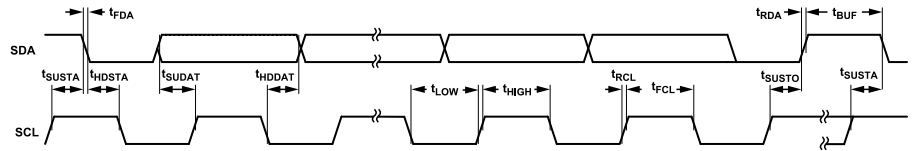


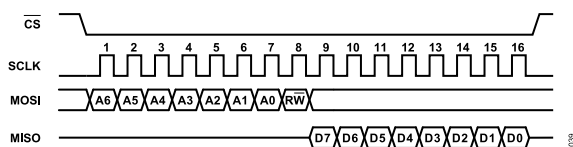*Figure 7. I²C Timing Diagram*
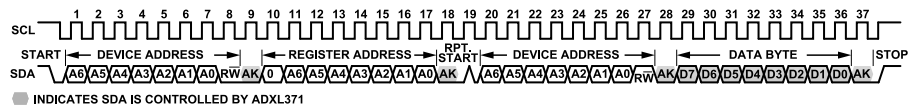


*Figure 8. I²C Timing Diagram, Single-Byte Read*
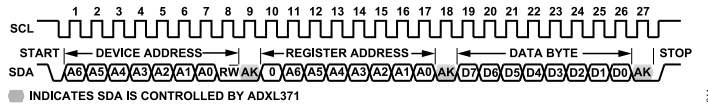


*Figure 9. I²C Timing Diagram, Single-Byte Write*
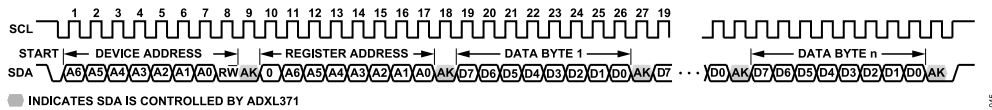


*Figure 10. I²C Timing Diagram, Multibyte Write*

## ABSOLUTE MAXIMUM RATINGS

*Table 4.*

| Parameter | Rating |
|---|---|
| Acceleration | |
| Any Axis, Unpowered | 10,000 $g$ for 0.1 ms |
| Any Axis, Powered | 10,000 $g$ for 0.1 ms |
| $V_S$ | −0.3 V to +3.6 V |
| $V_{DDI/O}$ | −0.3 V to +3.6 V |
| All Other Pins[1] | −0.3 V to $V_{DDIO}$ + 0.3 V |
| Output Short-Circuit Duration (Any Pin to Ground) | Indefinite |
| Temperature Range | |
| Storage | −50°C to +150°C |
| Powered | −40°C to +125°C |

[1] This value is limited to 3.6 V, maximum.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$θ_{JA}$ is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. $θ_{JC}$ is the junction to case thermal resistance.

*Table 5.*

| Package Type[1] | $θ_{JA}$ | $θ_{JC}$ | Unit | Device Weight |
|---|---|---|---|---|
| CC-16-4 | 150 | 85 | °C/W | 18 m$g$ |

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

### RECOMMENDED SOLDERING PROFILE

Figure 11 and Table 6 provide details about the recommended soldering profile.
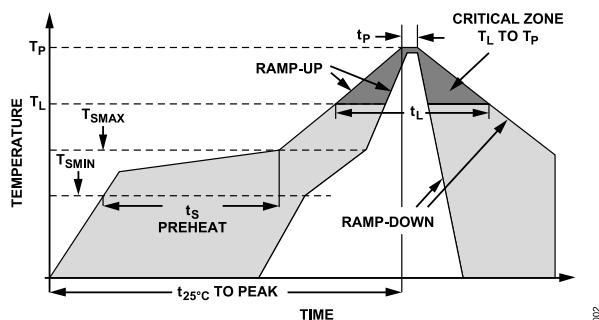


*Figure 11. Recommended Soldering Profile*

*Table 6. Recommended Soldering Profile*

| Profile Feature | Condition | |
|---|---|---|
| | **Sn63/Pb37** | **Pb-Free** |
| **Average Ramp Rate ($T_L$ to $T_P$)** | **3°C/sec max** | **3°C/sec max** |
| Preheat | | |
| Minimum Temperature ($T_{SMIN}$) | 100°C | 150°C |
| Maximum Temperature ($T_{SMAX}$) | 150°C | 200°C |
| Time ($T_{SMIN}$ to $T_{SMAX}$) ($t_S$) | 60 sec to 120 sec | 60 sec to 180 sec |
| $T_{SMAX}$ to $T_L$ Ramp-Up Rate | 3°C/sec max | 3°C/sec max |
| Time Maintained Above Liquidous ($T_L$) | | |
| Liquidous Temperature ($T_L$) | 183°C | 217°C |
| Time ($t_L$) | 60 sec to 150 sec | 60 sec to 150 sec |
| Peak Temperature ($T_P$) | 240 + 0/−5°C | 260 + 0/−5°C |
| Time Within 5°C of Actual Peak Temperature ($t_P$) | 10 sec to 30 sec | 20 sec to 40 sec |
| Ramp-Down Rate | 6°C/sec max | 6°C/sec max |
| Time 25°C to $T_P$ | 6 min max | 8 min max |

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

### ESD Ratings for ADXL371

*Table 7. ADXL371, 16-Terminal LGA*

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | 2000 | 1C |

### ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
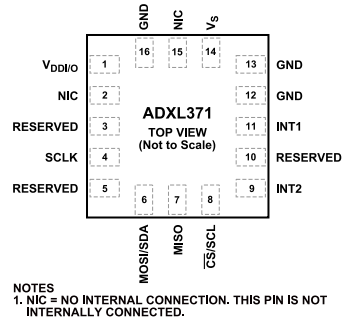


*Figure 12. Pin Configuration (Top View)*

*Table 8. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DDI/O}$ | Supply Voltage for Digital Input and Output. |
| 2 | NIC | No Internal Connection. This pin is not internally connected. |
| 3 | RESERVED | Reserved. This pin can be left unconnected or connected to GND. |
| 4 | SCLK | SPI Serial Communications Clock. |
| 5 | RESERVED | Reserved. This pin can be left unconnected or connected to GND. |
| 6 | MOSI/SDA | SPI Master Output, Slave Input (MOSI). I²C Serial Data (SDA). |
| 7 | MISO | SPI Master Input, Slave Output. |
| 8 | $\overline{CS}$/SCL | SPI Chip Select ($\overline{CS}$). I²C Serial Communications Clock (SCL). |
| 9 | INT2 | Interrupt 2 Output. This pin also serves as an input for synchronized sampling. |
| 10 | RESERVED | Reserved. This pin can be left unconnected or connected to GND. |
| 11 | INT1 | Interrupt 1 Output. This pin also serves as an input for external clocking. |
| 12 | GND | Ground. This pin must be connected to ground. |
| 13 | GND | Ground. This pin must be connected to ground. |
| 14 | $V_S$ | Supply Voltage. |
| 15 | NIC | No Internal Connection. This pin is not internally connected. |
| 16 | GND | Ground. This pin must be connected to ground. |

## TYPICAL PERFORMANCE CHARACTERISTICS
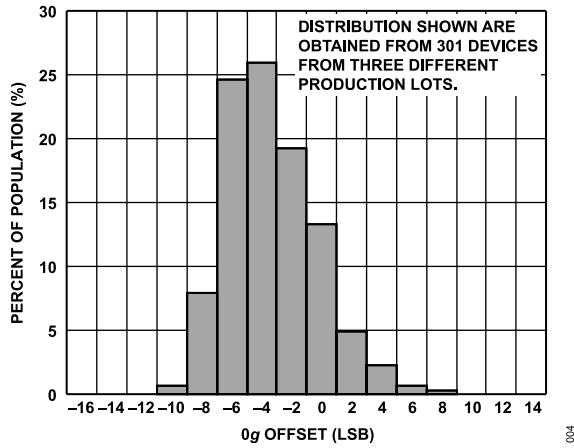


*Figure 13. X-Axis 0 g Offset (LSB) at 25°C, $V_S$ = 3.3 V*



*Figure 14. Y-Axis 0 g Offset (LSB) at 25°C, $V_S$ = 3.3 V*



*Figure 15. Z-Axis 1 g Offset (LSB) at 25°C, $V_S$ = 3.3 V*



*Figure 16. X-Axis Sensitivity at 25°C, $V_S$ = 3.3 V*
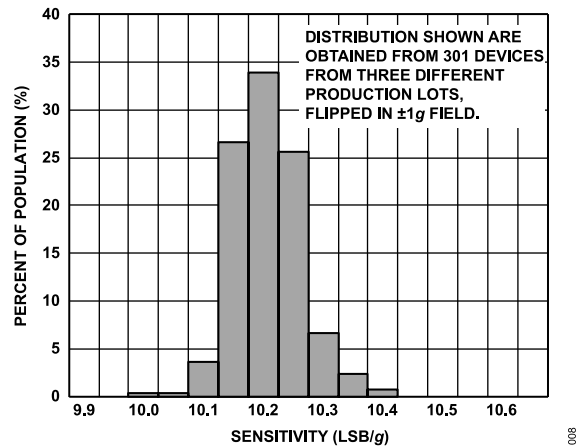


*Figure 17. Y-Axis Sensitivity at 25°C, $V_S$ = 3.3 V*
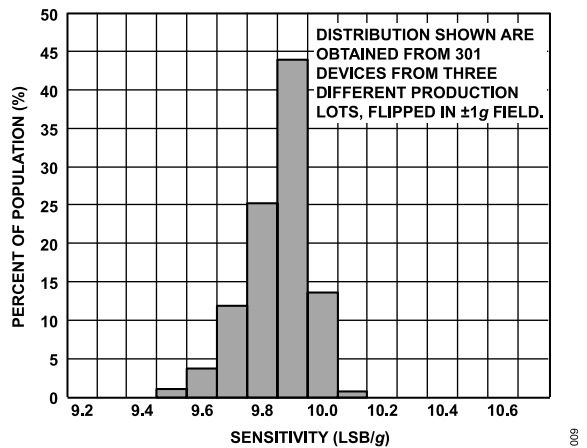


*Figure 18. Z-Axis Sensitivity at 25°C, $V_S$ = 3.3 V*

## TYPICAL PERFORMANCE CHARACTERISTICS



DISTRIBUTION SHOWN ARE OBTAINED FROM 301 DEVICES FROM THREE DIFFERENT PRODUCTION LOTS. TEMPERATURE COEFFICIENTS ARE MEASURED BEWTEEN −40°C TO +25°C AND BETWEEN +25°C TO +105°C. THE DISPLAYED TEMPERATURE IS THE LARGER OF THE TWO.
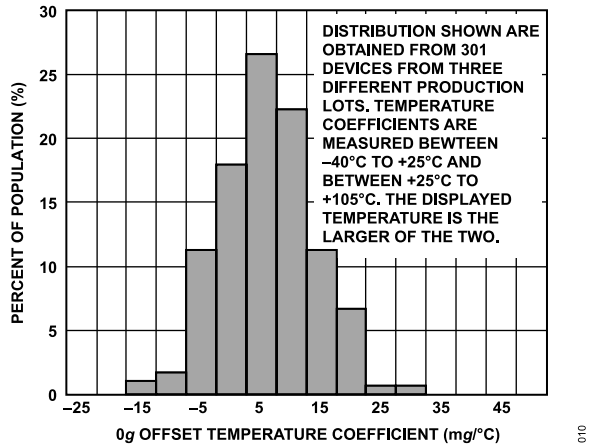
*Figure 19. X-Axis 0 g Offset Temperature Coefficient (mg/°C), $V_S$ = 3.3 V*



DISTRIBUTION SHOWN ARE OBTAINED FROM 301 DEVICES FROM THREE DIFFERENT PRODUCTION LOTS. TEMPERATURE COEFFICIENTS ARE MEASURED BEWTEEN −40°C TO +25°C AND BETWEEN +25°C TO +105°C. THE DISPLAYED TEMPERATURE IS THE LARGER OF THE TWO.
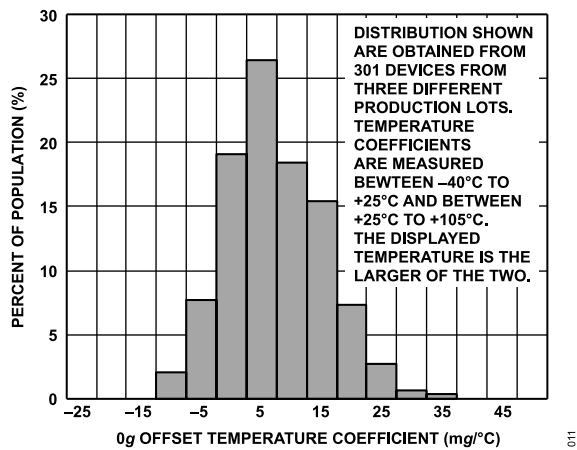
*Figure 20. Y-Axis 0 g Offset Temperature Coefficient (mg/°C), $V_S$ = 3.3 V*



DISTRIBUTION SHOWN ARE OBTAINED FROM 301 DEVICES FROM THREE DIFFERENT PRODUCTION LOTS. TEMPERATURE COEFFICIENTS ARE MEASURED BEWTEEN −40°C TO +25°C AND BETWEEN +25°C TO +105°C. THE DISPLAYED TEMPERATURE IS THE LARGER OF THE TWO.
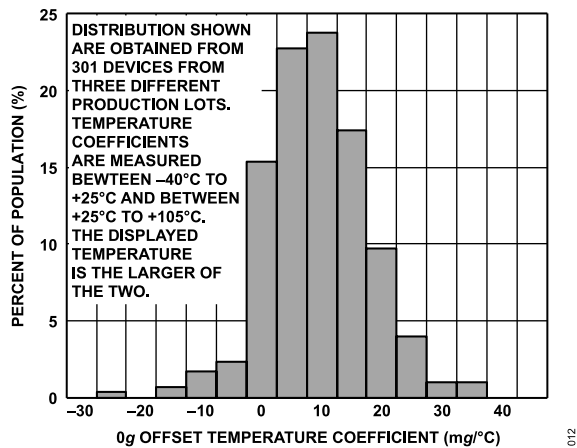
*Figure 21. Z-Axis 0 g Offset Temperature Coefficient, $V_S$ = 3.3 V*
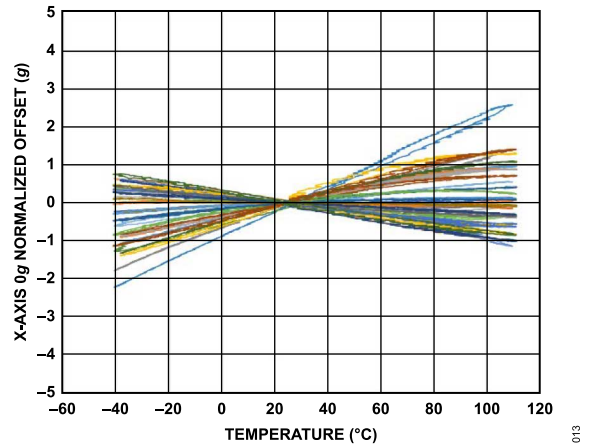


*Figure 22. X-Axis 0 g Normalized Offset vs. Temperature, 36 Devices Soldered to PCB, ODR = 2560 Hz*
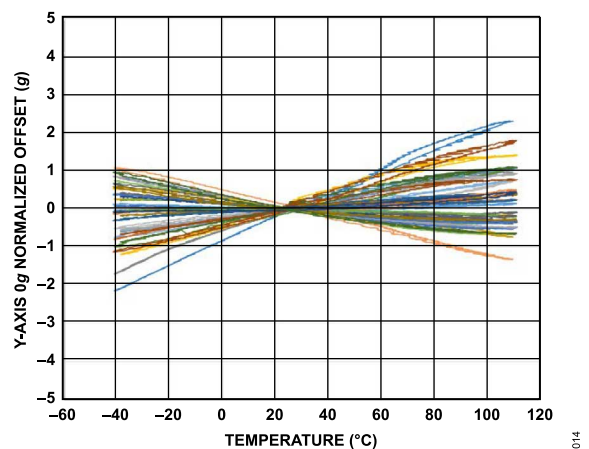


*Figure 23. Y-Axis 0 g Normalized Offset vs. Temperature, 36 Devices Soldered to PCB, ODR = 2560 Hz*
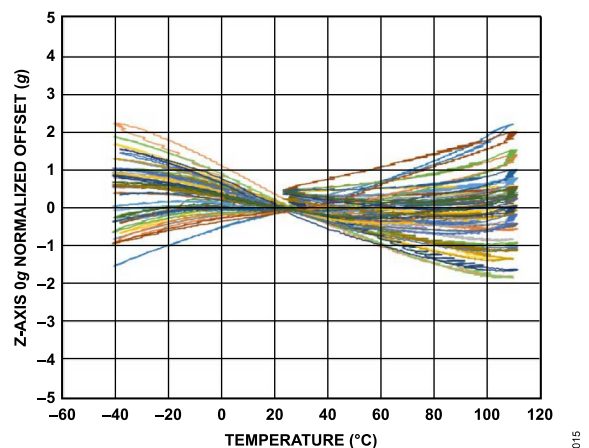


*Figure 24. Z-Axis 0 g Normalized Offset vs. Temperature, 36 Devices Soldered to PCB, ODR = 2560 Hz*

## TYPICAL PERFORMANCE CHARACTERISTICS
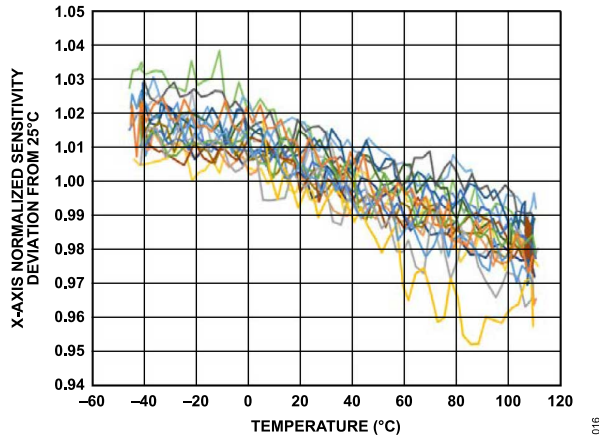


Figure 25. X-Axis Normalized Sensitivity Deviation from 25°C vs.
Temperature, 18 Devices Soldered to PCB, ODR = 2560 Hz
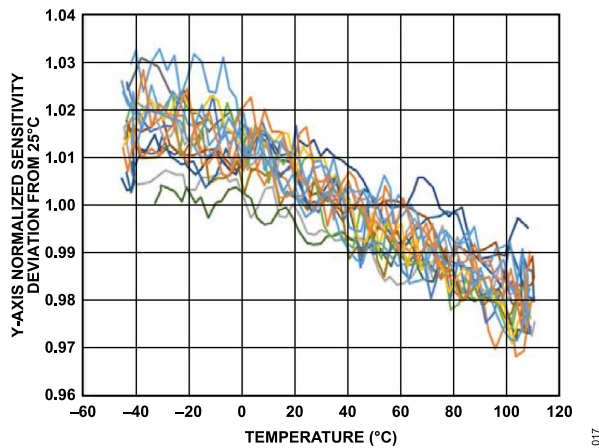


Figure 26. Y-Axis Normalized Sensitivity Deviation from 25°C vs.
Temperature, 17 Devices Soldered to PCB, ODR = 2560 Hz
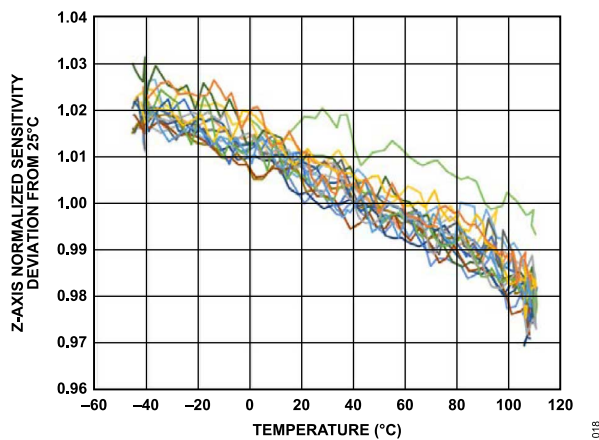


Figure 27. Z-Axis Normalized Sensitivity Deviation from 25°C vs.
Temperature, 18 Devices Soldered to PCB, ODR = 2560 Hz
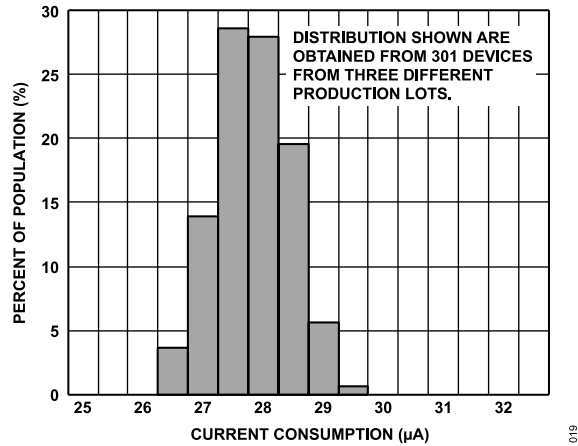


Figure 28. Current Consumption at 25°C, Normal Mode, 2560 Hz Output Data
Rate, $V_S$ = 3.3 V
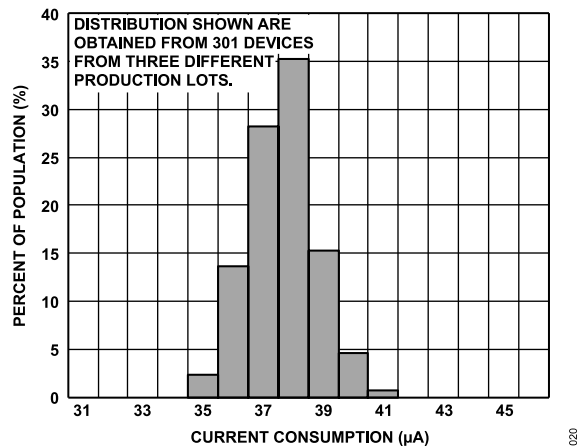


Figure 29. Current Consumption at 25°C, Low Noise Mode, 2560 Hz Output
Data Rate, $V_S$ = 3.3 V
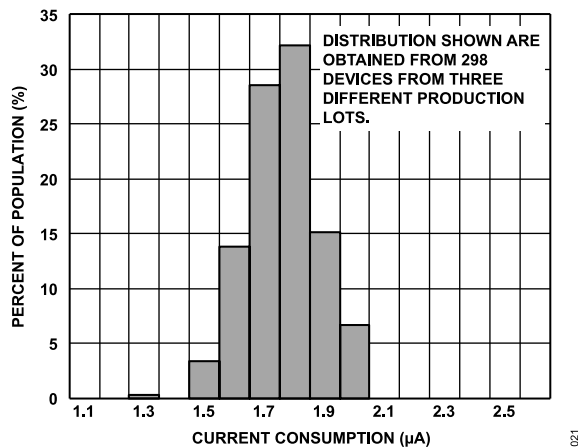


Figure 30. Current Consumption at 25°C, Instant On Mode, $V_S$ = 3.3 V

## TYPICAL PERFORMANCE CHARACTERISTICS
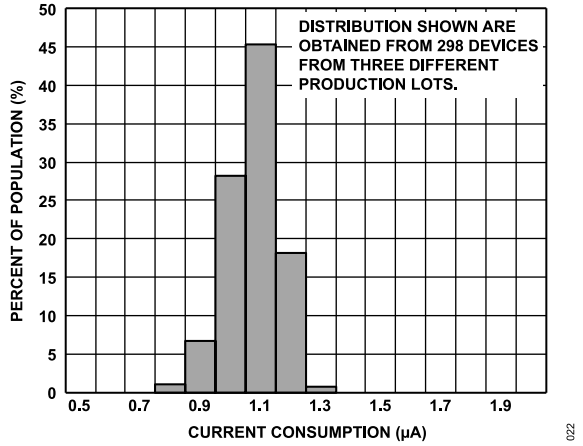


Figure 31. Current Consumption at 25°C, Wake-Up Mode, $V_S$ = 3.3 V



Figure 32. Clock Frequency Deviation from Ideal at 25°C, ODR = 2560 Hz, $V_S$ = 3.3 V



Figure 33. Clock Frequency Deviation from Ideal at 25°C, ODR = 5120 Hz, $V_S$ = 3.3 V



Figure 34. Current Consumption at 25°C, Standby Mode, $V_S$ = 3.3 V



Figure 35. Standby Current vs. Temperature
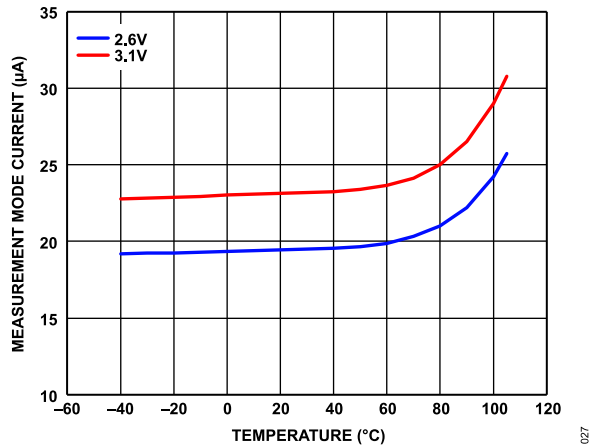


Figure 36. Measurement Mode Current vs. Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS
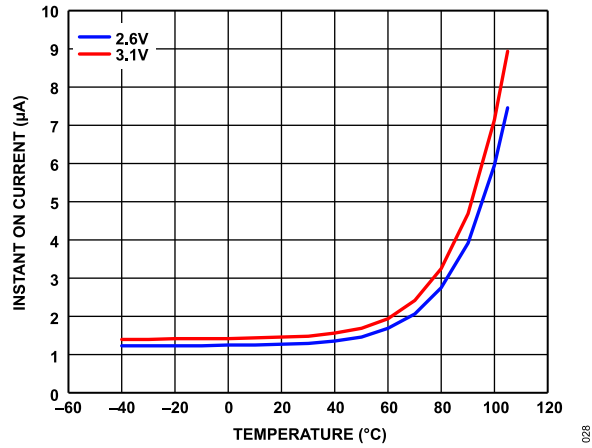


*Figure 37. Instant On Current vs. Temperature*
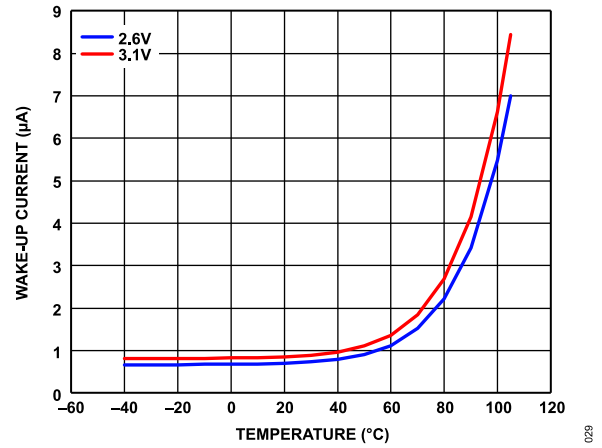


*Figure 38. Wake-Up Current vs. Temperature*

## THEORY OF OPERATION

The ADXL371 is a complete 3-axis acceleration measurement system that operates at extremely low power levels. Acceleration is reported digitally, and the device communicates via the SPI and I2C protocols. Built in digital logic enables autonomous operation and implements functions that enhance system level power savings.

## MECHANICAL DEVICE OPERATION

The moving component of the sensor is a polysilicon surface micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the structure and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase sensitive demodulation determines the magnitude and polarity of the acceleration.

## OPERATING MODES

The ADXL371 has three operating modes: a measurement mode for continuous, wide bandwidth sensing, an instant on mode for low power impact detection, and a wake-up mode for limited bandwidth, low $g$ activity detection. Measurement can be suspended by placing the device in standby mode.

### Measurement Mode

Measurement mode is the default operating mode of the ADXL371. In this mode, acceleration data is read continuously, and the accelerometer consumes 28 µA (typical) at an ODR of 2560 Hz when using a 3.3 V supply. Actual current consumption is dependent on the ODR chosen. All features described in this data sheet are available when operating the ADXL371 in this mode. After entering measurement mode, the first output value does not appear until after the filter settling time has passed. This time is selectable using the FILTER_SETTLE bit in the POWER_CTL register. See the Filter Settling Time section for more details.

### Instant On Mode

Instant on mode enables extremely low power impact detection. In this mode, the accelerometer constantly monitors the environment while consuming a low current of 1.7 µA (typical). When an event that exceeds an internal threshold is detected, the device switches into measurement mode to record the event. The target default threshold is 10 $g$ to 15 $g$, but it can vary. A register option allows the threshold to be increased to a target of 30 $g$ to 40 $g$ if the default threshold is too low.

To save power, no new digital acceleration data is made available until the accelerometer switches into normal operation. However, all registers have normal read and write functionality.

### Wake-Up Mode

Wake-up mode is ideal for simple detection of the presence or absence of motion at an extremely low power consumption. Wake-up mode is particularly useful for the implementation of a low $g$ motion activated on and off switch, allowing the rest of the system to be powered down until sustained activity is detected.

In wake-up mode, the device is powered down for a duration of time equal to the wake-up timer, set by the WAKEUP_RATE bits in the TIMING register, and then turns on for a duration equal to the filter settling time (see the Filter Settling Time section). The current drawn in this mode is determined by both of these parameters.

*Table 9. Wake-Up Current in µA at Different Wake-Up Timer and Filter Settings*

| Wake-Up Timer (ms) | Filter Settling Time | |
| --- | --- | --- |
| | 20 ms | 462.5 ms |
| 65 | 1.3 µA | 16.7 µA |
| 130 | 0.98 µA | 15 µA |
| 260 | 0.84 µA | 12.4 µA |
| 640 | 0.76 µA | 8.4 µA |
| 2560 | 0.71 µA | 3.5 µA |
| 5120 | 0.71 µA | 2.2 µA |
| 10,240 | 0.7 µA | 1.5 µA |
| 30,720 | 0.7 µA | 1 µA |

If motion is detected, the accelerometer can respond autonomously in several ways, depending on the device configuration, including the following:

▶ Switch into full bandwidth measurement mode
▶ Signal an interrupt to a microcontroller
▶ Wake up downstream circuitry

While in wake-up mode, all registers and the FIFO have normal read and write functionality, and real-time data can be read from the data registers at the reduced wake-up rate. However, no new data is stored in the FIFO during wake-up mode, and there are no interrupts available in wake-up mode.

### Standby

Placing the ADXL371 in standby mode suspends measurement and reduces current consumption to less than 100 nA. All interrupts are cleared, and no new interrupts are generated. The ADXL371 powers up in standby mode with all sensor functions turned off.

## BANDWIDTH

### Low-Pass Antialiasing Filter

High $g$ events often include acceleration content over a wide range of frequencies. The analog-to-digital converter (ADC) of the ADXL371 samples the input acceleration at the user selected ODR. In the absence of antialiasing filters, input signals whose frequency

## THEORY OF OPERATION

is more than half the ODR alias or that fold into the measurement bandwidth can lead to inaccurate measurements. To mitigate this inaccuracy, a four-pole, low-pass filter is provided at the input of the ADC. The filter bandwidth is user selectable, and the default bandwidth is 160 Hz. The maximum bandwidth is constrained to at most half of the ODR, to ensure that the Nyquist criteria is not violated.

### High-Pass Filter

The ADXL371 offers a one-pole, high-pass filter with a user selectable −3 dB frequency. Applications that do not require dc acceleration measurements can use the high-pass filter to minimize constant or slow varying offset errors including initial bias, bias drift due to temperature, and bias drift due to supply voltage.

The high-pass filter is a first-order infinite impulse response (IIR) filter. Table 10 lists the available −3 dB frequencies, which are user selectable and dependent on the output data rate. The high-pass and low-pass filters can be used simultaneously to set up a band-pass option.

Table 10. High-Pass Filter −3 dB Corner Frequencies

| Setting | ODR (Hz) | | | | |
| --- | --- | --- | --- | --- | --- |
| | 5120 | 2560 | 1280 | 640 | 320 |
| 00 | 24.38 | 12.19 | 6.09 | 3.05 | 1.52 |
| 01 | 12.46 | 6.23 | 3.11 | 1.55 | 0.78 |
| 10 | 6.30 | 3.15 | 1.58 | 0.78 | 0.39 |
| 11 | 3.17 | 1.58 | 0.79 | 0.39 | 0.19 |

### Filter Settling Time

After entering measurement mode, the first output value does not appear until after the filter settling time has passed. This time is selectable using the FILTER_SETTLE bit in the POWER_CTL register. The recommended (and default) settling time to acquire valid data when using either the high-pass filter or the low-pass activity detect filter is 462.5 ms. The filter settling time of 20 ms is ideal for when both the high-pass filter and low-pass activity detect filter are disabled.

### Selectable ODR

The ADXL371 can report acceleration data at 320 Hz, 640 Hz, 1280 Hz, 2560 Hz, or 5120 Hz. The ODR is user selectable, and the default is 320 Hz. If the user selects an antialiasing filter bandwidth greater than half the ODR, the device defaults the bandwidth to 50% of the ODR. Increasing or decreasing the ODR increases or decreases the current consumption, accordingly, as shown in Figure 39.
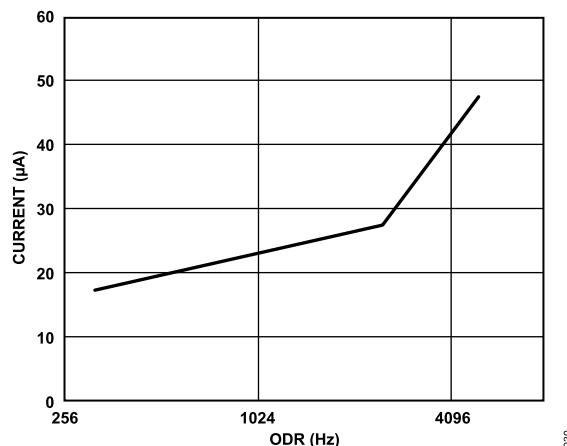


Figure 39. Typical Measurement Mode Current vs. ODR

## POWER/NOISE TRADE-OFF

The noise performance of the ADXL371 in normal operation, typically 6.5 m$g$/√Hz at 2560 Hz ODR and 1280 Hz bandwidth, is adequate for most applications, depending on bandwidth and the desired resolution. For cases where lower noise is needed, the ADXL371 provides a lower noise operating mode that trades reduced noise for a somewhat higher current consumption. In all cases, operating at a higher bandwidth setting increases the rms noise and operating at a lower bandwidth settling decreases the rms noise. Table 11 lists the current consumption and noise densities obtained for normal operation and the lower noise mode at a typical 3.3 V supply.

Table 11. Noise and Current Consumption for $V_S$ = 3.3 V

| Mode | Typical Noise Bandwidth (m$g$/√Hz) | Typical Current Consumption (μA) |
| --- | --- | --- |
| Normal Operation[1] | 6.5 | 28 |
| Low Noise[1] | 5.5 | 37 |

[1]  $V_S$ = 3.3 V, ODR = 2560 Hz, and bandwidth = 1280 Hz.

## POWER SAVINGS

The digital interface of the ADXL371 is implemented with system level power savings in mind. The following features enhance power savings:

► Burst reads and writes reduce the number of SPI communication cycles required to configure the device and retrieve data.
► Concurrent operation of activity and inactivity detection enables set it and forget it operation. Loop modes further reduce communications power by enabling the clearing of interrupts without processor intervention.
► The FIFO is implemented such that consecutive samples can be read continuously via a multibyte read of unlimited length. Thus, one FIFO read instruction can clear the entire contents of the FIFO. The ADXL371 FIFO construction also allows the use of direct memory access (DMA) to read the FIFO contents.

## AUTONOMOUS EVENT DETECTION

### ACTIVITY AND INACTIVITY

The ADXL371 features built in logic that detects activity (acceleration more than a user set threshold) and inactivity (acceleration less than a user set threshold). Activity and inactivity events can be used as triggers to manage the accelerometer operating mode, trigger an interrupt to a host processor, and/or autonomously drive a motion switch.

Detection of an activity or inactivity event is indicated in the STATUS2 register and can be configured to generate an interrupt. In addition, the activity status of the device, that is, whether it is moving or stationary, is indicated by the AWAKE bit (STATUS register), described in the Using the AWAKE Bit section.

Activity and inactivity detection can be used when the accelerometer is in either measurement mode or wake-up mode. However, the activity and inactivity interrupts are not available in wake-up mode because the device is inherently looking for activity in this mode, and any changes to the activity or inactivity detection features must be made while the device is in standby mode.

### Low-Pass Activity Detect Filter

The ADXL371 combines high $g$ impact detection and low $g$ movement detection in one device. For low $g$ detection, an internal low-pass filter with a −3 dB corner of approximately 8 Hz averages data to reduce the rms noise, allowing accurate detection of activity or inactivity thresholds as low as 500 m$g$. For high $g$ impact detection, the low-pass activity detect filter can be turned off through a register setting. When using both the low-pass activity detect filter and the high-pass filter, the user must select a high-pass filter corner that does not exceed 8 Hz. Otherwise, activity detection data is severely attenuated.

### Activity Detection

An activity event is detected when acceleration in at least one enabled axis remains above a specified threshold for a specified time. Enabled axes, thresholds, and time are user selected. Each axis has its own activity threshold, but the activity timer is shared among all three axes. When multiple axes are selected, an over-threshold event on any one enabled axis triggers the activity detection.

### Referenced and Absolute Configurations

Activity detection can be configured as referenced or absolute mode for all axes through the ACT_REF bit in the THRESH_ACT_X_L register.

When using absolute activity detection, acceleration samples are compared directly to a user set threshold to determine whether motion is present. For example, if a threshold of 0.5 $g$ is set and the acceleration on the z-axis is 1 $g$ longer than the user defined activity time, the activity status asserts.

In many applications, it is advantageous for activity detection to be based not on an absolute threshold but on a deviation from a reference point or orientation. The referenced activity detection is particularly useful because it removes the effect on activity detection of the static 1 $g$ imposed by gravity as well as any static offset errors, which can be up to several $g$. In absolute activity detection, when the threshold is set to less than 1 $g$, activity is immediately detected in this case.

In the referenced configuration, activity is detected when acceleration samples are more than an internally defined reference by a user defined amount for the user defined amount of time, as described by

$Abs(Acceleration − Reference) > Threshold$

where $Abs$ is the absolute value.

Consequently, activity is detected only when the acceleration has deviated sufficiently from the initial orientation. The default setting for the accelerometer is in absolute mode. After it is placed in referenced mode through the appropriate register setting, the reference for activity detection is calculated as soon as the full bandwidth measurement mode is turned on. To reset the reference, it is necessary to put the device back into absolute mode and then back into referenced mode. The new reference is set as soon as the device enters full bandwidth measurement mode again. If using both activity and inactivity detection in referenced mode, both must be set back to absolute mode before the reference can be reset.

### Activity Timer

Ideally, the intent of activity detection is to wake up a system only when motion is intentional, ignoring noise or small, unintentional movements. In addition to being sensitive to low $g$ events, the ADXL371 activity detection algorithm is robust in filtering out undesired triggers.

The ADXL371 activity detection functionality includes a timer to filter out unwanted motion and ensure that only sustained motion is recognized as activity. The timer period depends on the ODR selected. At 2560 Hz and under, it is approximately 8.25 ms, and at 5120 Hz, it is approximately 2.06 ms. For activity detection to trigger, above threshold activity must be sustained for a time equal to the number of activity timer periods specified in the activity time register. For example, a setting of 10 in this register means that above threshold activity must be sustained for 82.5 ms at 2560 Hz ODR. A register value of zero results in single sample activity detection. The maximum allowable activity time is approximately 2.1 sec (or 0.53 sec at 5120 Hz ODR). Note that the activity timer is operational in measurement mode only.

### Activity Detection in Wake-Up Mode

If activity detection is enabled while the device is in wake-up mode, the device uses single sample activity detection, no matter the activity time register setting. If activity is detected, the device automatically returns to full bandwidth measurement mode. However, the activity interrupt is not generated unless the activity time setting

## AUTONOMOUS EVENT DETECTION

is zero. If it is not zero, after entering measurement mode, the interrupt is not generated until the device sees sustained activity for the amount of time given in the activity time register. The awake interrupt automatically goes high upon entering measurement mode if the device is in default mode or autosleep mode. If it is in linked or loop mode (but not autosleep), it is linked to the activity interrupt, which behaves as previously mentioned.

After the device automatically enters measurement mode due to activity detection, if autosleep is not on, it must be placed manually back into wake-up mode.

### Inactivity Detection

An inactivity event is detected when acceleration in all enabled axes remains less than a specified threshold for a specified time. Enabled axes, threshold, and time are user selected. Each axis has its own inactivity threshold, but the inactivity timer is shared among all three axes. When multiple axes are selected, all enabled axes must stay less than the threshold for the required amount of time to trigger inactivity detection.

### Referenced and Absolute Configurations

Inactivity detection is also configurable as referenced or absolute through the INACT_REF bit in the THRESH_INACT_X_L register. When using absolute inactivity detection, acceleration samples are compared directly to a user set threshold for the user set time to determine the absence of motion. Inactivity is detected when enough consecutive samples are all less than the threshold.

When using referenced inactivity detection, inactivity is detected when acceleration samples are within a user specified amount from an internally defined reference for a user defined amount of time.

$Abs(Acceleration - Reference) < Threshold$

Referenced inactivity, like referenced activity, is particularly useful for eliminating the effects of the static acceleration due to gravity, as well as other static offsets. With absolute inactivity, if the inactivity threshold is set lower than 1 $g$, a device resting motionless may never detect inactivity. With referenced inactivity, the same device under the same configuration detects inactivity. The default setting for the accelerometer is in absolute mode. After it is placed in referenced mode through the appropriate register setting, the reference for inactivity detection is calculated as soon as full bandwidth measurement mode is turned on. To reset the reference, it is necessary to put the device back into absolute mode and then back into referenced mode. The new reference is set as soon as the device enters full bandwidth measurement mode again. If using both inactivity and activity detection in referenced mode, both must be set back to absolute mode before the reference can be reset.

### Inactivity Timer

The ADXL371 inactivity detect functionality includes a timer to allow detection of sustained inactivity. The timer period depends on the

ODR selected. At 2560 Hz and under, it is approximately 32.5 ms regardless of ODR. For inactivity detection to trigger, under threshold inactivity must be sustained for a time equal to the number of inactivity timer periods specified in the inactivity time registers. For example, a setting of 10 in these registers means that under threshold inactivity must be sustained for 325 ms. A value of zero in these registers results in single sample, inactivity detection. The maximum allowable inactivity time is approximately 35.5 minutes.

### Linking Activity and Inactivity Detection

When in measurement mode or wake-up mode, the activity and inactivity detection functions can be used concurrently and processed manually by a host processor, or these functions can be configured to interact in several other ways, such as those described in the following sections.

### Default Mode

In default mode, activity and inactivity detection are both available simultaneously, and all interrupts must be serviced by a host processor. That is, a processor must read each interrupt before it is cleared and can be used again. Refer to the Interrupts section for information on clearing interrupts.

The flowchart in Figure 40 illustrates default mode operation.



NOTES
1. THE AWAKE BIT DEFAULTS TO 1 WHEN ACTIVITY AND INACTIVITY ARE NOT LINKED.
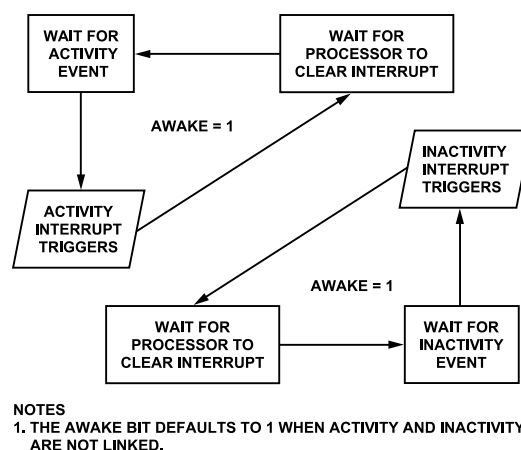
Figure 40. Flowchart Illustrating Activity and Inactivity Operation in Default Mode

### Linked Mode

In linked mode, activity and inactivity detection are linked to each other so that only one of the functions is enabled at any given time. As soon as activity is detected, the device is assumed to be moving (or awake) and stops looking for activity. Rather, inactivity is expected as the next event. Therefore, only inactivity detection operates.

Similarly, when inactivity is detected, the device is assumed to be stationary (or asleep). Thus, activity is expected as the next event. Therefore, only activity detection operates.

## AUTONOMOUS EVENT DETECTION

In linked mode, each interrupt must be serviced by a host processor before the next interrupt is enabled.

The flowchart in Figure 41 illustrates linked mode operation.
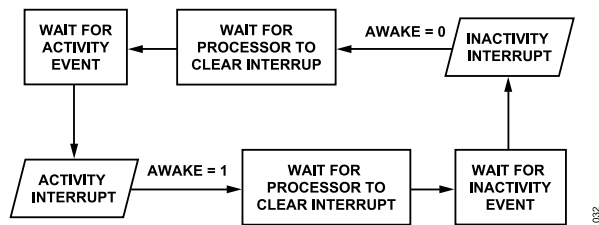


*Figure 41. Flowchart Illustrating Activity and Inactivity Operation in Linked Mode*

### Loop Mode

In loop mode, motion detection operates as described in the Linked Mode section, but interrupts do not need to be serviced by a host processor. This configuration simplifies the implementation of commonly used motion detection and enhances power savings by reducing the amount of power used in bus communication.

The flowchart in Figure 42 illustrates loop mode operation.
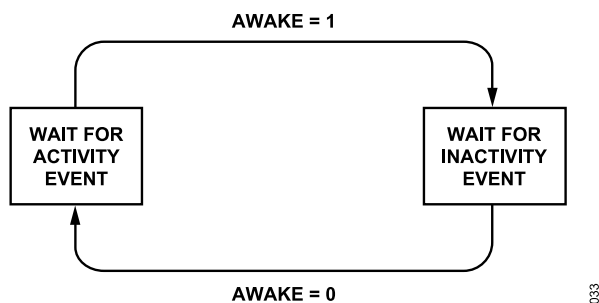


*Figure 42. Flowchart Illustrating Activity and Inactivity Operation in Loop Mode*

### Autosleep

If autosleep is selected, after the device is placed in wake-up mode (see the Wake-Up Mode section), it automatically sets to loop mode and begins looking for activity. When activity is detected, the device automatically enters measurement mode and immediately begins looking for inactivity. When inactivity is detected, the device automatically re-enters wake-up mode. Note that the device must be manually placed in wake-up mode before autosleep can begin functioning. It does not automatically enter wake-up mode if the device is started up manually in measurement mode.

### Using the AWAKE Bit

The AWAKE bit is a status bit that indicates whether the ADXL371 is awake or asleep. In default mode or autosleep mode, the AWAKE bit is high whenever the device is in measurement mode. In linked or loop mode, the AWAKE bit is high whenever the device

experiences an activity condition, and it is low when the device experiences an inactivity condition.

The awake signal can be mapped to the INT1 pin or the INT2 pin allowing the pin to serve as a status output to connect or disconnect power to downstream circuitry based on the awake status of the accelerometer. Used in conjunction with loop mode, this configuration implements a simple, autonomous motion activated switch.

If the turn-on time of downstream circuitry can be tolerated, this motion switch configuration can save significant system level power by eliminating the standby current consumption of the remainder of the application circuit. This standby current can often exceed the full operating current of the ADXL371.

## MOTION WARNING

In addition to the activity threshold previously described, the ADXL371 offers a secondary threshold. This second threshold, the motion warning threshold, can be set independently of the activity threshold. It does not have any functionality related to autosleep, linked, or loop mode, or the device awake status. The purpose of the motion warning functionality is to issue a notification to the system, via the status bit and/or interrupt, that the observed acceleration has exceeded the second threshold. It is controlled by the THRESH_ACT2_x_x registers, and by the ACTIVITY2 interrupt, which is sent only to the INT2 pin. Each axis has its own motion warning threshold. However, the motion warning activity interrupt does not have an activity timer. It is only used for single sample, activity detection. The motion warning threshold also shares the same referenced and absolute configuration as the primary activity detection.

## IMPACT DETECTION FEATURES

Impact detection applications often require high *g* and high bandwidth acceleration measurements, and the ADXL371 is designed with these applications in mind. Several features are included that target impact detection and aim to simplify the system design.

### WIDE BANDWIDTH

An impact is a transient event that produces an acceleration pulse with frequency content over a wide range. A sufficiently wide bandwidth is needed to capture the impact event because lowering bandwidth has the effect of reducing the magnitude of the recorded signal, resulting in measurement inaccuracy.

The ADXL371 can operate with bandwidths of up to 2560 Hz at extremely low power levels. A steep filter roll-off is also useful for effective suppression of out of band content, and the ADXL371 incorporates a four-pole, low-pass antialiasing filter for this purpose.

### INSTANT ON IMPACT DETECTION

The ADXL371 instant on mode is an ultra low power mode that continuously monitors the environment for impact events that exceed a built in threshold. When an impact is detected, the device switches into full measurement mode and captures the impact profile.

No digital data is available in this mode of operation. The user can configure the device to detect an impact between a threshold level of either 10 *g* to 15 *g* or 30 *g* to 40 *g* by using the INSTANT_ON_THRESH bit in the POWER_CTL register. When an impact beyond the selected threshold is detected, the ADXL371 switches to full bandwidth measurement mode and begins outputting digital data.
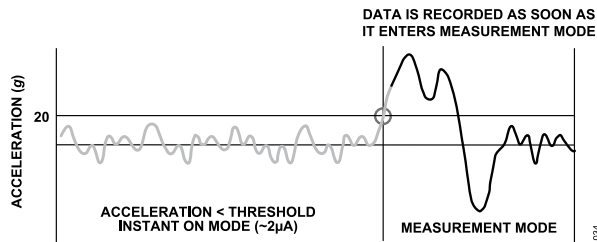


*Figure 43. Instant On Mode Using Default Threshold*

After the accelerometer is in full bandwidth measurement mode, the mode must be set back into instant on mode manually. The mode cannot return to instant on mode automatically.

### CAPTURING IMPACT EVENTS

In certain applications, a single (3-axis) acceleration sample at the peak of an impact event contains sufficient information about the event, and the full acceleration history is not required. For these applications, the ADXL371 provides the capability to store only the peak acceleration of each impact event. The ADXL371 peak detection function considers an impact event as an acceleration signal that occurs within an activity interrupt and the next inactivity interrupt. The peak of an impact event is defined as the x, y, and z acceleration sample that has the highest magnitude of all

other values within an impact event, as shown in Figure 44. The magnitude of each sample set is calculated as $x^2 + y^2 + z^2$.
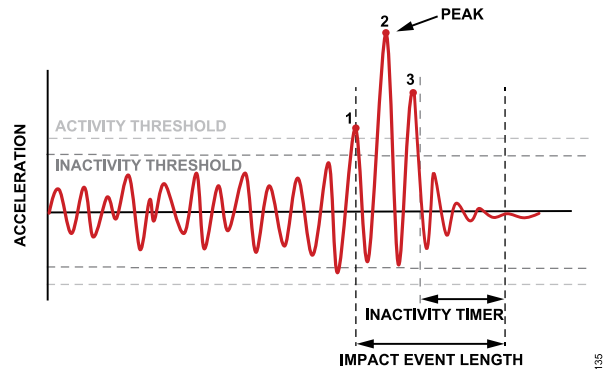


*Figure 44. Capturing Impact Events*

The peak detection feature stores the peak acceleration in the MAXPEAK_x_x registers (Register 0x15 to Register 0x1A). When these values are read out of the registers, the register data is cleared, and the device begins looking for a new peak. Furthermore, if MAXPEAK_x_x registers were not read after an impact event and another impact event with a higher peak occurs, the MAXPEAK_x_x registers are automatically updated with the higher peak acceleration values. On the contrary, if the next peak magnitude is lower than the current peak stored in MAXPEAK_x_x registers, the MAXPEAK_x_x registers are not updated. In the example of Figure 45, if the MAXPEAK_x_x registers are read after Impact Event 4, their values correspond to the peak detected during Impact Event 3, which was the highest peak of all four impact events.
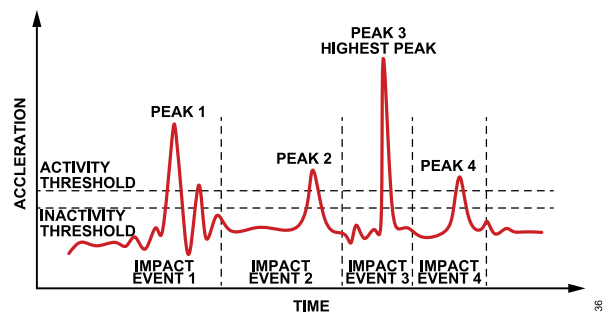


*Figure 45. Capturing Highest Peak Within Multiple Impact Events*

Follow these steps to enable peak detection:

1. Configure the FIFO_CTL register into peak detect mode (b0011100X to Register 0x3A).
2. Set the desired activity threshold and time settings (Register 0x23 to Register 0x29).
3. Set the desired inactivity threshold and time settings (Register 0x2A to Register 0x31).
4. Set the activity mode to linked or loop mode (Register 0x3E).

The FIFO provides even more flexibility to the peak detection feature, allowing its use in applications that require to keep record

## IMPACT DETECTION FEATURES

of the peak of all impact events that occurred within a period of time, with minimal intervention from the host processor. To do so, follow these steps:

1. Configure the FIFO_CTL register into peak detect mode and stream mode (b0011101X to Register 0x3A).
2. Set the desired activity threshold and time settings (Register 0x23 to Register 0x29).
3. Set the desired inactivity threshold and time settings (Register 0x2A to Register 0x31).
4. Set the activity mode to linked or loop mode (Register 0x3E).

Always read acceleration data from MAXPEAK_x_x registers and from the FIFO memory using multibyte transfer to ensure a concurrent and complete set of x, y, and z acceleration data is read.

### Limitations

The user must be aware that the ADXL371 cannot properly capture impact events of higher frequency than the user selected bandwidth. As a rule, the ADXL371 must be able to capture at least two samples from the moment the activity interrupt is triggered to the moment the peak acceleration occurs. If this requirement is not met, significantly lower acceleration values than the actual peak, or even zeros, may be stored in the MAXPEAK_x_x registers.

The peak detection function determines the peak of an event by comparing the sum square of each set of x, y, and z acceleration samples within an impact event. The sum square is performed internally using 7-bit multipliers, and because the acceleration data is 12-bit resolution, a maximum error of approximately ±3 $g$ can occur on the determination of the peak.

## FIFO

### BENEFITS OF THE FIFO

The FIFO buffer is an important feature in ultralow power applications in two ways: system level power savings and data recording/event context.

### System Level Power Savings

Appropriate use of the FIFO enables system level power savings by enabling the host processor to sleep for extended periods while the accelerometer autonomously collects data. Alternatively, using the FIFO to collect data can unburden the host while it tends to other tasks.

### Data Recording/Event Context

The FIFO can be used in a triggered mode to record all data leading up to an activity detection event, thereby providing context for the event. In the case of a system that identifies impact events, for example, the accelerometer can keep the entire system off while it stores acceleration data in its FIFO and looks for an activity event. When the impact event occurs, data collected prior to the event is frozen in the FIFO. The accelerometer can now wake the rest of the system and transfer this data to the host processor, thereby providing context for the impact event.

Generally, the more context available, the more intelligent decisions a system can achieve, making a deep FIFO especially useful. For example, the ADXL371 FIFO can store up to 512 1-axis samples at 400 Hz ODR to provide a 1.28 sec window, or 170 3-axis samples at 3200 Hz to provide a 50 ms window, which is a typical duration for impact events.

### USING THE FIFO

The FIFO is a 512-sample memory buffer that can save power, unburden the host processor, and autonomously record data.

FIFO operation is configured via Register 0x39 and Register 0x3A. The 512 FIFO samples can be allotted in several ways, such as the following:

- 170 sample sets of concurrent 3-axis data
- 256 sample sets of concurrent 2-axis data (user selectable)
- 512 sample sets of single-axis data
- 170 sets of impact event peak (x, y, z)

All FIFO modes must be configured while in standby mode. When reading data from multiple axes from the FIFO, to ensure that data is not overwritten and stored out of order, at least one sample set must be left in the FIFO after every read (therefore, a set of 3-axis data must have 169 samples at most).

The FIFO operates in one of the following four modes: FIFO disabled, oldest saved mode (first N), stream mode (last N), and triggered mode.

### FIFO Disabled

When the FIFO is disabled, no new data is stored in it, and any data already in it is cleared.

The FIFO is disabled by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b00.

### Oldest Saved Mode (First N)

In oldest saved mode, the FIFO accumulates data until it is full and then stops. After reading the data, the FIFO must be disabled and re-enabled to save a new set of data. One possible use case for this mode is to enable it right after entering instant on mode. After a shock is detected, the data immediately stores in the FIFO to be read whenever convenient.

The FIFO is placed into oldest saved mode by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b11.

### Stream Mode (Last N)

In stream mode, the FIFO always contains the most recent data. The oldest sample is discarded when space is needed to make room for a newer sample.

Stream mode is useful for unburdening a host processor. The processor can tend to other tasks while data is being collected in the FIFO. When the FIFO fills to a certain number of samples (specified by the FIFO_SAMPLES register along with Bit 0 in the FIFO_CTL register), it triggers a watermark interrupt (if this interrupt is enabled). At this point, the host processor can read the contents of the entire FIFO and then return to its other tasks as the FIFO fills again.

The FIFO is placed into stream mode by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b01.

### Triggered Mode

In triggered mode, the FIFO operates as in stream mode until an activity detection event, after which it saves the samples surrounding that event. The operation is similar to a one-time run trigger on an oscilloscope. The number of samples to be saved after the activity event is specified in FIFO_SAMPLES (Register 0x39[7:0], along with Bit 0 in the FIFO_CTL register, Register 0x3A). For example if the FIFO_SAMPLE is set to 12, there are 500 samples before the trigger and 12 after the trigger. The trigger can be reset by clearing the activity interrupt and reading all 512 locations of the FIFO. If this is not complete, future FIFO data reads may contain invalid data. Place the FIFO into triggered mode by setting the FIFO_MODE bits in the FIFO_CTL register (Register 0x3A) to 0b10.

### RETRIEVING DATA FROM FIFO

Access FIFO data by reading the FIFO_DATA register. A multibyte read to this register does not auto-increment the address, and

## FIFO

instead continues to pop data from the FIFO. Data is left justified and formatted as shown in Table 12.

When reading data, the most significant byte (Bits[B15:B8]) is read first, followed by the least significant byte (Bits[B7:B0]).

Bits[B15:B4] represent the 12-bit, twos complement acceleration data. Bit 0 serves as a series start indicator: only the first data byte of a series contains a 1 in this bit, and the remaining items contain a 0.

*Table 12. FIFO Buffer Data Format—Bits[B15:B8]*

| B15 (MSB) | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
|-----------|-----|-----|-----|-----|-----|-----|-----|
| Data | | | | | | | |

*Table 13. FIFO Buffer Data Format—Bits[B7:B0]*

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| Data | | | | Reserved | | | Series start indicator |

## INTERRUPTS

Several of the built in functions of the ADXL371 can trigger interrupts to alert the host processor of certain status conditions. The functionality of these interrupts is described in this section.

### INTERRUPT PINS

Interrupts can be mapped to either (or both) of two designated output pins, INT1 and INT2, by setting the appropriate bits in the INT1_MAP register and INT2_MAP register, respectively. All functions can be used simultaneously. If multiple interrupts are mapped to one pin, the OR combination of the interrupts determines the status of the pin.

If no functions are mapped to an interrupt pin, that pin is automatically configured to a high impedance (high-Z) state. The INTx pins are also placed in the high-Z state upon a reset.

When a certain status condition is detected, the INTx pin that condition is mapped to activates. The configuration of the INTx pin is active high by default so when the pin is activated, it goes high. However, this configuration can be switched to active low by setting the INTx_LOW bit in the appropriate INTx_MAP register.

The INTx pins can connect to the interrupt input of a host processor where interrupts are responded to with an interrupt routine. Because multiple functions can be mapped to the same pin, the STATUS register can determine which condition caused the interrupt to trigger.

Interrupts are cleared in several of the following ways:

▶ Reading the STATUS2 register clears ACTIVITY and INACT interrupts. However, if activity detection is operating in default mode, and the activity or inactivity timers are set to 0, the only way to clear the activity or inactivity bits, respectively, is to set the device into standby mode and restart full bandwidth measurement mode.
▶ Reading the STATUS2 register clears the ACTIVITY2 interrupt. It is not required to set the device back in standby mode to clear this interrupt, no matter what value is set for the activity timer.
▶ Reading from the data registers clears the DATA_RDY interrupt.
▶ Reading enough data from the FIFO buffer so that interrupt conditions are no longer met, and then reading the STATUS register (Register 0x04) clears the FIFO_RDY, FIFO_FULL, and FIFO_OVR interrupts.

Both INTx pins are push-pull low impedance pins with an output impedance of about 500 Ω (typical) and digital output specifications as shown in Table 14. Both INTx pins have bus keepers that hold the pins to a valid logic state when the pins are in high impedance mode.

To prevent interrupts from being falsely triggered during configuration, disable interrupts while their settings, such as thresholds, timings, or other values, are configured.

### Alternate Functions

The INT1 and INT2 pins can be configured for use as input pins instead of for signaling interrupts. INT1 is used as an external clock input when the EXT_CLK bit in the TIMING register is set. INT2 is used as the trigger input for synchronized sampling when the EXT_SYNC bit in the TIMING register is set. One or both of these alternate functions can be used concurrently. However, if an interrupt pin is used for its alternate function, the INTx pin cannot be used simultaneously to signal interrupts.

### TYPES OF INTERRUPTS

### Activity and Inactivity Interrupts

The ACTIVITY bit and INACT bit are set when activity and inactivity are detected, respectively. Detection procedures and criteria are described in the Autonomous Event Detection section.

### Data Ready Interrupt

The DATA_RDY bit is set when new valid data is available, and it is cleared when no new data is available.

The DATA_RDY bit does not set while any of the data registers are being read. If DATA_RDY = 0 prior to a register read and new data becomes available during the register read, DATA_RDY remains 0 until the read completes and then only sets to 1.

If DATA_RDY = 1 prior to a register read, it is cleared at the start of the register read.

If DATA_RDY = 1 prior to a register read and new data becomes available during the register read, DATA_RDY is cleared to 0 at the start of the register read and remains 0 throughout the read. When the read completes, DATA_RDY is set to 1.

### FIFO Interrupts

### FIFO Watermark

The FIFO_FULL bit is set when the number of samples stored in the FIFO is equal to or exceeds the number specified in FIFO_SAMPLES (Register 0x39 together with Bit 0 in the FIFO_CTL register). The FIFO_FULL bit is cleared automatically when enough samples are read from the FIFO, such that the number of samples remaining is lower than that specified.

If the number of FIFO samples is set to 0, the watermark interrupt is set. To avoid unexpectedly triggering this interrupt, the default value of the FIFO_SAMPLES register is 0x80.

### FIFO Ready

The FIFO_RDY bit is set when there is at least one valid sample available in the FIFO output buffer. This bit is cleared when no valid data is available in the FIFO. In FIFO triggered mode, it is only set

## INTERRUPTS

after the activity interrupt is detected, and the data surrounding the event is saved in the FIFO.

### Overrun

The FIFO_OVR bit is set when the FIFO has overrun or overflowed, such that new data replaces unread data, which may indicate a full FIFO that has not yet been emptied or a clocking error caused by

a slow SPI transaction. If the FIFO is configured to oldest saved mode, an overrun event indicates that there is insufficient space available for a new sample.

The FIFO_OVR bit is cleared when both the contents of the FIFO and the STATUS register are read. It is also cleared when the FIFO is disabled.

*Table 14. Interrupt Pin Digital Output*

| Parameter | Test Conditions | Limit[1] Min | Limit[1] Max | Unit |
|---|---|---|---|---|
| Digital Output | | | | |
| Low Level Output Voltage ($V_{OL}$) | $I_{OL}$ = 500 µA | | $0.2 \times V_{DDI/O}$ | V |
| High Level Output Voltage ($V_{OH}$) | $I_{OH}$ = −300 µA | $0.8 \times V_{DDI/O}$ | | V |
| Low Level Output Current ($I_{OL}$) | $V_{OL} = V_{OL,\ MAX}$ | 500 | | µA |
| High Level Output Current ($I_{OH}$) | $V_{OH} = V_{OH,\ MIN}$ | | −300 | µA |
| Pin Capacitance | $f_{IN}$ = 1 MHz, $V_{IN}$ = 2.0 V | | 8 | pF |
| Rise/Fall Time | | | | |
| Rise Time ($t_R$)[2] | $C_{LOAD}$ = 150 pF | | 210 | ns |
| Fall Time ($t_F$)[3] | $C_{LOAD}$ = 150 pF | | 150 | ns |

[1]  Limits based on characterization results, not production tested.

[2]  Rise time is measured as the transition time from $V_{OL,\ MAX}$ to $V_{OH,\ MIN}$ of the interrupt pin.

[3]  Fall time is measured as the transition time from $V_{OH,\ MIN}$ to $V_{OL,\ MAX}$ of the interrupt pin.

## ADDITIONAL FEATURES

### USING AN EXTERNAL CLOCK

When operating at 2560 Hz ODR or lower, the ADXL371 has a built in 307.2 kHz (typical) clock that, by default, serves as the time base for internal operations. At 5120 Hz ODR, this clock speed increases to 614.4 kHz (typical). If desired, an external clock can be provided instead, for either improved clock frequency accuracy or for control of the output data rate. To use an external clock, set the EXT_CLK bit (Bit 1) in the TIMING register (Register 0x3D) and apply a clock to the INT1 pin.

The external clock can operate at the nominal 307.2 kHz or slower (when using ODR ≤ 2560 Hz), or 614.4 kHz or slower (when using ODR = 5120 Hz) to allow the user to achieve any desired output data rate. Lower external clock rates must be used with caution because it may result in aliasing of high frequency signals that may be present in certain applications.

ODR and bandwidth scale proportionally with the clock. The ADXL371 provides a discrete number of options for ODR. ODRs other than those provided are achieved by selecting an appropriate clock frequency. For example, to achieve a 2048 Hz ODR, use the 2560 Hz setting with a clock frequency that is 80% of nominal, or 245.76 kHz. Bandwidth also scales by the same ratio, therefore, if a 320 Hz bandwidth is selected, the resulting bandwidth is 256 Hz.

### SYNCHRONIZED DATA SAMPLING

For applications that require a precisely timed acceleration measurement, the ADXL371 features an option to synchronize acceleration sampling to an external trigger. The EXT_SYNC bit in the TIMING register enables this feature. When the EXT_SYNC bit is set to 1, the INT2 pin automatically reconfigures for use as the sync trigger input.

When external triggering is enabled, it is up to the system designer to ensure that the sampling frequency meets system requirements. Sampling too infrequently causes aliasing. Noise can be lowered by oversampling. However, sampling at too high a frequency may not allow enough time for the accelerometer to process the acceleration data and convert it to valid digital output data.

When the Nyquist criterion is met, signal integrity is maintained. An internal antialiasing filter is available in the ADXL371 and can assist the system designer in maintaining signal integrity. To prevent aliasing, set the filter bandwidth to a frequency no greater than half the sampling rate. For example, when sampling at 1280 Hz, set the filter bandwidth to no higher than 640 Hz.

Because of internal timing requirements, the maximum allowable external trigger frequencies are as follows:

▶ 1-axis data = 3100 Hz
▶ 2-axis data = 2700 Hz
▶ 3-axis data = 2200 Hz

These values are doubled when an ODR rate of 5120 Hz is selected. Additionally, the trigger signal applied to the INT2 pin must meet the following criteria:

▶ The trigger signal must be active high.
▶ The pulse width of the trigger signal must be at least 53 µs.
▶ The minimum sampling frequency is set only by system requirements. Samples need not be polled at any minimum rate. However, if samples are polled at a rate lower than the bandwidth set by the antialiasing filter, aliasing may occur.

The EXT_SYNC is an active high signal. Due to the asynchronous nature of the internal clock and external sync, there may be a one ODR clock cycle difference between consecutive external sync pulses. The external sync sets the ODR of the system. For example, if sending an external sync at a 2 kHz rate, all three axes (if enabled) are sampled in that 2 kHz window.

### SELF TEST

When the self test function is invoked, an electrostatic force is applied to the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and the acceleration experienced by the device increases because of this force. The high-pass filter is automatically disabled for this feature.

#### Self Test Procedure

The self test function is enabled via the ST bit in the SELF_TEST register, Register 0x40. The ST_DONE bit indicates when the test is completed. Figure 46 describes the self test profile from when ST is set until ST_DONE goes high, which typically takes around 200 ms. The self test passes if |ΔST| is greater than 5 LSB.
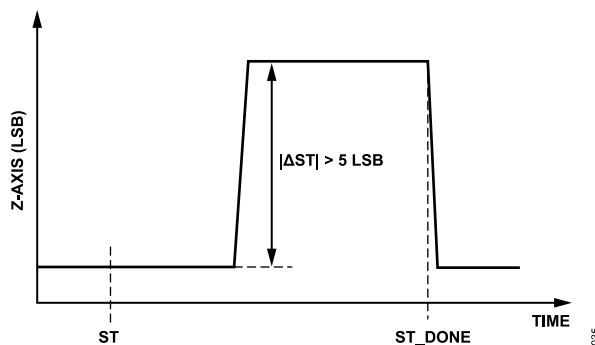


*Figure 46. Self Test Waveform*

The recommended procedure for using the self test functionality is as follows:

1. Ensure that the low-pass activity filter is enabled.
2. Place the device in measurement mode.
3. Wait until the filter settling time passes.
4. Start the self test by setting the ST bit in the SELF_TEST register (Register 0x40).

## ADDITIONAL FEATURES

5. Read the acceleration data from the z-axis (Register 0x0C and Register 0x0D) and store the data until the self test completes (ST_DONE goes high).
6. Average the first 50 ms of data right after ST is set.
7. Average the last 50 ms of data right before ST_DONE goes high.
8. If the absolute value of the difference between the two averaged values is greater than 5 LSB, the self test passes.

During the deviation of the z-axis, the x-axis and y-axis also show deviation, which is normal. However, the outputs of the x-axis and y-axis cannot be used to qualify pass or fail of the self test.

## USER REGISTER PROTECTION

The ADXL371 includes user register protection for single event upsets (SEUs). An SEU is a change of state caused by ions or electromagnetic radiation striking a sensitive node in a microelectronic device. The state change is a result of the free charge created by ionization in or close to an important node of a logic element (for example, a memory bit). The SEU itself is not considered permanently damaging to transistor or circuit functionality, but it can create erroneous register values. The registers protected from SEU are Register 0x20 to Register 0x3F.

Protection is implemented via a 99-bit error correcting (Hamming type) code and detects both single bit and double bit errors. The check bits are recomputed any time a write to any of the protected registers occurs. At any time, if the stored version of the check bits is not in agreement with the current check bit calculation, the ERR_USER_REGS status bit is set.

The ERR_USER_REGS bit in the STATUS register starts high when set on an unconfigured device and clears after the first register write.

## USER OFFSET TRIMS

The ADXL371 has a 4-bit offset trim for each axis that allows users to add positive or negative offset to the default static acceleration values and correct any deviations from ideal that may result as a consequence of varying the operating parameters of the device. The offset trims have a full-scale range of approximately ±60 LSB with a trim profile, as shown in Figure 47.
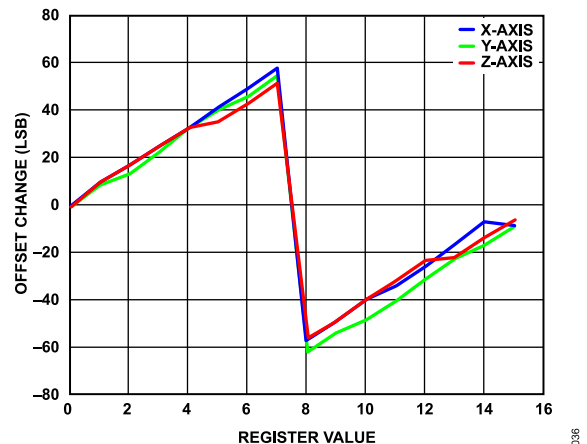


*Figure 47. User Offset Trim Profile*

## SERIAL COMMUNICATIONS

### SERIAL INTERFACE

The ADXL371 is designed to communicate in either the SPI or the I$^2$C protocol. It autodetects the format being used, requiring no configuration control to select the format.

### SPI Protocol

The timing scheme is as follows: phase (CPHA) = polarity (CPOL) = 0. The ADXL371 supports a SCLK frequency up to 10 MHz. Wire the ADXL371 for SPI communication as shown in Figure 48. For successful communication, follow the logic thresholds and timing parameters in Table 1. The command structure for the read register and write register are shown in Figure 2 and Figure 3, respectively. The read and write register commands support multibyte (burst) read/write access. The waveform diagrams for multibyte read and write commands are shown in Figure 4 and Figure 5, respectively.

Ignore data transmitted from the ADXL371 to the master device during writes to the ADXL371.
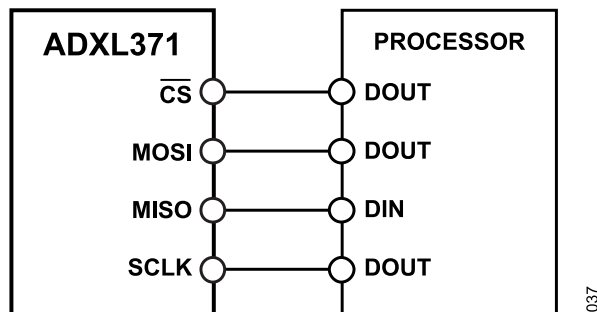


*Figure 48. 4-Wire SPI Connection Diagram*

### I$^2$C Protocol

The ADXL371 supports standard (100 kHz), fast (up to 1 MHz), and high speed (up to 3.4 MHz) data transfer modes if the bus parameters given in Table 1 and shown in Figure 1 are met. There is no minimum SCL frequency, with the exception that when reading data, the clock must be fast enough to read an entire sample set before new data overwrites it. Single-byte or multibyte reads and writes are supported. With the MISO pin low, the I$^2$C address for the device is 0x1D, and an alternate I$^2$C address of 0x53 can be chosen by pulling the MISO pin high.

There are no internal pull-up or pull-down resistors for any unused pins. Therefore, there is no known state or default state for the MISO and SCLK pins if left floating or unconnected. It is a requirement that SCLK be connected to ground when communicating to the ADXL371 using the I$^2$C.

Due to communication speed limitations, the maximum output data rate when using about 6 kHz I$^2$C is 640 Hz and scales linearly with I$^2$C communication speed. Operation at an output data rate higher than the recommended maximum can result in an undesirable effect on the acceleration data, including missing samples or additional noise.

If other devices are connected to the same I$^2$C bus, the nominal operating voltage level of these other devices cannot exceed V$_{DDI/O}$ by more than 0.3 V. External pull-up resistors (R$_P$) are necessary for proper I$^2$C operation. Single-byte or multibyte reads and writes are supported, as shown from Figure 2 to Figure 4.
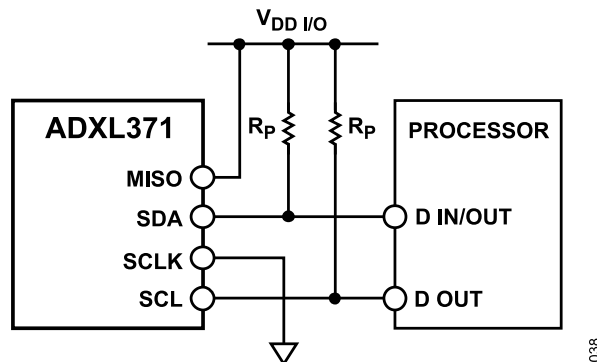


*Figure 49. I$^2$C Connection Diagram (ADXL371 Device ID = 0x53)*

### MULTIBYTE TRANSFERS

Both the SPI and I$^2$C protocols support multibyte transfers, also known as burst transfers. A register read or write begins with the address specified in the command and autoincrements for each additional byte in the transfer. Always read acceleration data using multibyte transfers to ensure that a concurrent and complete set of x-, y-, and z-acceleration data is read.

The FIFO runs on the serial port clock during FIFO reads and can sustain bursting at the SPI clock rate as long as the SPI clock is 1 MHz or faster.

The address auto-increment function is disabled when the FIFO address is used, which is so that data can be read continuously from the FIFO as a multibyte transaction. In cases where the starting address of a multibyte transaction is less than the FIFO address, the address auto-increments until the FIFO address is reached, and then it stops at the FIFO address.

When writing data to the ADXL371 in I$^2$C mode, the no acknowledge (NACK) bit never generates. Instead, the acknowledge (ACK) bit is sent after every received byte because it is not known how many bytes are included in the transfer. The master decides how many bytes are sent and ends the transaction with the stop condition.

### INVALID ADDRESSES AND ADDRESS FOLDING

The ADXL371 has a 6-bit address bus, mapping only 104 registers in the possible 256 register address space. The addresses do not fold to repeat the registers at addresses above 0x104. Attempted access to register addresses above 0x104 are mapped to the invalid register at 0x67 and have no functional effect.

## SERIAL COMMUNICATIONS

Register 0x00 to Register 0x41 are for customer access, as described in Table 15. Register 0x42 to Register 0x67 are reserved for factory use.

# ADXL371

## REGISTER MAP

*Table 15. Register Map*

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | DEVID_AD | [7:0] | DEVID_AD | | | | | | | | 0xAD | R |
| 0x01 | DEVID_MST | [7:0] | DEVID_MST | | | | | | | | 0x1D | R |
| 0x02 | PARTID | [7:0] | DEVID_PRODUCT | | | | | | | | 0xFA | R |
| 0x03 | REVID | [7:0] | REVID | | | | | | | | 0xFB | R |
| 0x04 | STATUS | [7:0] | ERR_USER_REGS | AWAKE | USER_NVM_BUSY | RESERVED | FIFO_OVR | FIFO_FULL | FIFO_RDY | DATA_RDY | 0xA0 | R |
| 0x05 | STATUS2 | [7:0] | RESERVED | ACTIVITY2 | ACTIVITY | INACT | RESERVED | | | | 0x00 | R |
| 0x06 | FIFO_ENTRIES2 | [7:0] | RESERVED | | | | | | FIFO_ENTRIES[9:8] | | 0x00 | R |
| 0x07 | FIFO_ENTRIES | [7:0] | FIFO_ENTRIES[7:0] | | | | | | | | 0x00 | R |
| 0x08 | XDATA_H | [7:0] | XDATA[11:4] | | | | | | | | 0x00 | R |
| 0x09 | XDATA_L | [7:0] | XDATA[3:0] | | | | RESERVED | | | | 0x00 | R |
| 0x0A | YDATA_H | [7:0] | YDATA[11:4] | | | | | | | | 0x00 | R |
| 0x0B | YDATA_L | [7:0] | YDATA[3:0] | | | | RESERVED | | | | 0x00 | R |
| 0x0C | ZDATA_H | [7:0] | ZDATA[11:4] | | | | | | | | 0x00 | R |
| 0x0D | ZDATA_L | [7:0] | ZDATA[3:0] | | | | RESERVED | | | | 0x00 | R |
| 0x15 | MAXPEAK_X_H | [7:0] | MAXPEAK_X[11:4] | | | | | | | | 0x00 | R |
| 0x16 | MAXPEAK_X_L | [7:0] | MAXPEAK_X[3:0] | | | | RESERVED | | | | 0x00 | R |
| 0x17 | MAXPEAK_Y_H | [7:0] | MAXPEAK_Y[11:4] | | | | | | | | 0x00 | R |
| 0x18 | MAXPEAK_Y_L | [7:0] | MAXPEAK_Y[3:0] | | | | RESERVED | | | | 0x00 | R |
| 0x19 | MAXPEAK_Z_H | [7:0] | MAXPEAK_Z[11:4] | | | | | | | | 0x00 | R |
| 0x1A | MAXPEAK_Z_L | [7:0] | MAXPEAK_Z[3:0] | | | | RESERVED | | | | 0x00 | R |
| 0x20 | OFFSET_X | [7:0] | RESERVED | | | | OFFSET_X | | | | 0x00 | R/W |
| 0x21 | OFFSET_Y | [7:0] | RESERVED | | | | OFFSET_Y | | | | 0x00 | R/W |
| 0x22 | OFFSET_Z | [7:0] | RESERVED | | | | OFFSET_Z | | | | 0x00 | R/W |
| 0x23 | THRESH_ACT_X_H | [7:0] | THRESH_ACT_X[10:3] | | | | | | | | 0x00 | R/W |
| 0x24 | THRESH_ACT_X_L | [7:0] | THRESH_ACT_X[2:0] | | | RESERVED | | | ACT_REF | ACT_X_EN | 0x00 | R/W |
| 0x25 | THRESH_ACT_Y_H | [7:0] | THRESH_ACT_Y[10:3] | | | | | | | | 0x00 | R/W |
| 0x26 | THRESH_ACT_Y_L | [7:0] | THRESH_ACT_Y[2:0] | | | RESERVED | | | | ACT_Y_EN | 0x00 | R/W |
| 0x27 | THRESH_ACT_Z_H | [7:0] | THRESH_ACT_Z[10:3] | | | | | | | | 0x00 | R/W |
| 0x28 | THRESH_ACT_Z_L | [7:0] | THRESH_ACT_Z[2:0] | | | RESERVED | | | | ACT_Z_EN | 0x00 | R/W |
| 0x29 | TIME_ACT | [7:0] | ACT_COUNT | | | | | | | | 0x00 | R/W |
| 0x2A | THRESH_INACT_X_H | [7:0] | THRESH_INACT_X[10:3] | | | | | | | | 0x00 | R/W |
| 0x2B | THRESH_INACT_X_L | [7:0] | THRESH_INACT_X[2:0] | | | RESERVED | | | INACT_REF | INACT_X_EN | 0x00 | R/W |
| 0x2C | THRESH_INACT_Y_H | [7:0] | THRESH_INACT_Y[10:3] | | | | | | | | 0x00 | R/W |
| 0x2D | THRESH_INACT_Y_L | [7:0] | THRESH_INACT_Y[2:0] | | | RESERVED | | | | INACT_Y_EN | 0x00 | R/W |
| 0x2E | THRESH_INACT_Z_H | [7:0] | THRESH_INACT_Z[10:3] | | | | | | | | 0x00 | R/W |
| 0x2F | THRESH_INACT_Z_L | [7:0] | THRESH_INACT_Z[2:0] | | | RESERVED | | | | INACT_Z_EN | 0x00 | R/W |
| 0x30 | TIME_INACT_H | [7:0] | INACT_COUNT[15:8] | | | | | | | | 0x00 | R/W |
| 0x31 | TIME_INACT_L | [7:0] | INACT_COUNT[7:0] | | | | | | | | 0x00 | R/W |
| 0x32 | THRESH_ACT2_X_H | [7:0] | THRESH_ACT2_X[10:3] | | | | | | | | 0x00 | R/W |

## REGISTER MAP

*Table 15. Register Map*

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x33 | THRESH_ACT2_X_L | [7:0] | THRESH_ACT2_X[2:0] | | | RESERVED | | | ACT2_REF | ACT2_X_EN | 0x00 | R/W |
| 0x34 | THRESH_ACT2_Y_H | [7:0] | THRESH_ACT2_Y[10:3] | | | | | | | | 0x00 | R/W |
| 0x35 | THRESH_ACT2_Y_L | [7:0] | THRESH_ACT2_Y[2:0] | | | RESERVED | | | | ACT2_Y_EN | 0x00 | R/W |
| 0x36 | THRESH_ACT2_Z_H | [7:0] | THRESH_ACT2_Z[10:3] | | | | | | | | 0x00 | R/W |
| 0x37 | THRESH_ACT2_Z_L | [7:0] | THRESH_ACT2_Z[2:0] | | | RESERVED | | | | ACT2_Z_EN | 0x00 | R/W |
| 0x38 | HPF | [7:0] | RESERVED | | | | | | HPF_CORNER | | 0x00 | R/W |
| 0x39 | FIFO_SAMPLES | [7:0] | FIFO_SAMPLES[7:0] | | | | | | | | 0x80 | R/W |
| 0x3A | FIFO_CTL | [7:0] | RESERVED | | FIFO_FORMAT | | | FIFO_MODE | | FIFO_SAMPLES[8] | 0x00 | R/W |
| 0x3B | INT1_MAP | [7:0] | INT1_LOW | AWAKE_INT1 | ACT_INT1 | INACT_INT1 | FIFO_OVR_INT1 | FIFO_FULL_INT1 | FIFO_RDY_INT1 | DATA_RDY_INT1 | 0x00 | R/W |
| 0x3C | INT2_MAP | [7:0] | INT2_LOW | AWAKE_INT2 | ACT2_INT2 | INACT_INT2 | FIFO_OVR_INT2 | FIFO_FULL_INT2 | FIFO_RDY_INT2 | DATA_RDY_INT2 | 0x00 | R/W |
| 0x3D | TIMING | [7:0] | ODR | | | WAKEUP_RATE | | | EXT_CLK | EXT_SYNC | 0x00 | R/W |
| 0x3E | MEASURE | [7:0] | USER_OR_DISABLE | AUTO-SLEEP | LINKLOOP | | LOW_NOISE | BANDWIDTH | | | 0x00 | R/W |
| 0x3F | POWER_CTL | [7:0] | I2C_HSM_EN | RESERVED | INSTANT_ON_THRESH | FILTER_SETTLE | LPF_DISABLE | HPF_DISABLE | MODE | | 0x00 | R/W |
| 0x40 | SELF_TEST | [7:0] | RESERVED | | | | | | ST_DONE | ST | 0x00 | R/W |
| 0x41 | RESET | [7:0] | RESET | | | | | | | | 0x00 | W |
| 0x42 | FIFO_DATA | [7:0] | FIFO_DATA | | | | | | | | 0x00 | R |

## REGISTER DETAILS

### ANALOG DEVICES ID REGISTER

**Address: 0x00, Reset: 0xAD, Name: DEVID_AD**

This register contains the Analog Devices, Inc., ID, 0xAD.

```
7  6  5  4  3  2  1  0
1  0  1  0  1  1  0  1
```
[7:0] DEVID_AD (R)
Analog Devices ID, 0xAD.
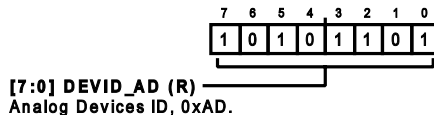
*Table 16. Bit Descriptions for DEVID_AD*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | DEVID_AD | | Analog Devices ID, 0xAD. | 0xAD | R |

### ANALOG DEVICES MEMS ID REGISTER

**Address: 0x01, Reset: 0x1D, Name: DEVID_MST**

This register contains the Analog Devices MEMS ID, 0x1D.

```
7  6  5  4  3  2  1  0
0  0  0  1  1  1  0  1
```
[7:0] DEVID_MST (R)
Analog Devices MEMS ID, 0x1D.
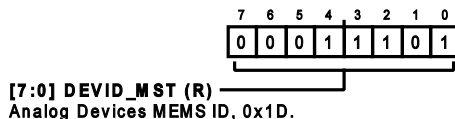
*Table 17. Bit Descriptions for DEVID_MST*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | DEVID_MST | | Analog Devices MEMS ID, 0x1D. | 0x1D | R |

### DEVICE ID REGISTER

**Address: 0x02, Reset: 0xFA, Name: PARTID**

This register contains the device ID, 0xFA (372 octal).

```
7  6  5  4  3  2  1  0
1  1  1  1  1  0  1  0
```
[7:0] DEVID_PRODUCT (R)
Device ID, 0xFA (372 Octal).
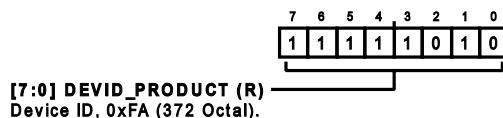
*Table 18. Bit Descriptions for PARTID*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | DEVID_PRODUCT | | Device ID, 0xFA (372 Octal). | 0xFA | R |

### PRODUCT REVISION ID REGISTER

**Address: 0x03, Reset: 0xFB, Name: REVID**

This register contains the mask revision ID, beginning with 0x00 and incrementing for each subsequent revision.

```
7  6  5  4  3  2  1  0
1  1  1  1  1  0  1  1
```
[7:0] REVID (R)
Mask revision.
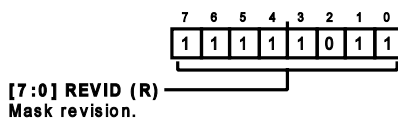
## REGISTER DETAILS

*Table 19. Bit Descriptions for REVID*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | REVID | | Mask revision. | 0xFB | R |

## STATUS REGISTER

**Address: 0x04, Reset: 0xA0, Name: STATUS**

This register includes the following bits that describe various conditions of the ADXL371.
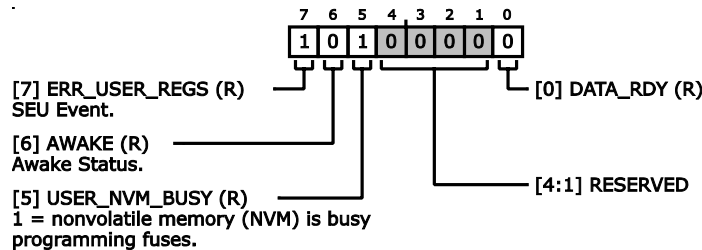


*Table 20. Bit Descriptions for STATUS*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | ERR_USER_REGS | | SEU Event. An SEU event is detected in a user register. | 0x1 | R |
| 6 | AWAKE | | Awake Status. Activity detected, and the device is moving. | 0x0 | R |
| 5 | USER_NVM_BUSY | | 1 = nonvolatile memory (NVM) is busy programming fuses. | 0x1 | R |
| [4:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | DATA_RDY | | Status is high after the full data set completes. A complete x, y, and z measurement was made, and results can be read. | 0x0 | R |

## ACTIVITY STATUS REGISTER

**Address: 0x05, Reset: 0x00, Name: STATUS2**
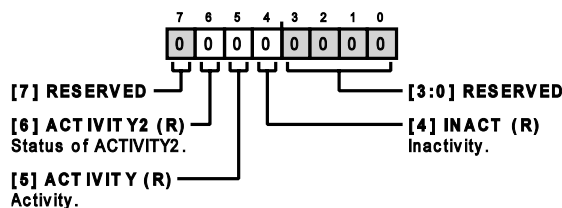


*Table 21. Bit Descriptions for STATUS2*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | RESERVED | | Reserved. | 0x0 | R |
| 6 | ACTIVITY2 | | Status of ACTIVITY2. | 0x0 | R |
| 5 | ACTIVITY | | Activity. Activity is detected. | 0x0 | R |
| 4 | INACT | | Inactivity. Inactivity is detected. | 0x0 | R |
| [3:0] | RESERVED | | Reserved. | 0x0 | R |

## X-AXIS DATA REGISTER, MSB

**Address: 0x08, Reset: 0x00, Name: XDATA_H**

These two registers contain the x-axis acceleration data. Data is left justified and formatted as twos complement. XDATA_H contains the eight MSBs, and XDATA_L contains the four LSBs of the 12-bit value.

## REGISTER DETAILS

[7:0] XDATA[11:4] (R)
X-axis data.
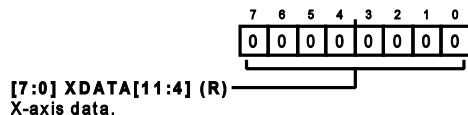
*Table 22. Bit Descriptions for XDATA_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | XDATA[11:4] | | X-axis data. | 0x0 | R |

## X-AXIS DATA REGISTER, LSB

**Address: 0x09, Reset: 0x00, Name: XDATA_L**

[7:4] XDATA[3:0] (R)
X-axis data.
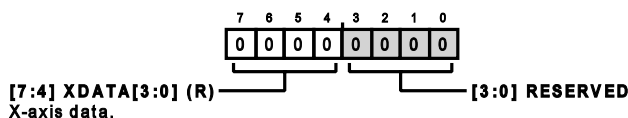
[3:0] RESERVED

*Table 23. Bit Descriptions for XDATA_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | XDATA[3:0] | | X-axis data. | 0x0 | R |
| [3:0] | RESERVED | | Reserved. | 0x0 | R |

## Y-AXIS DATA REGISTER, MSB

**Address: 0x0A, Reset: 0x00, Name: YDATA_H**

The YDATA_H and YDATA_L registers contain the y-axis, LSB acceleration data. Data is left justified and formatted as twos complement. YDATA_H contains the eight MSBs, and YDATA_L contains the four LSBs of the 12-bit value.

YDATA_L latches on a read of YDATA_H to ensure data integrity.

[7:0] YDATA[11:4] (R)
Y-axis data.
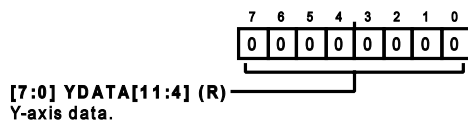
*Table 24. Bit Descriptions for YDATA_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | YDATA[11:4] | | Y-axis data. | 0x0 | R |

## Y-AXIS DATA REGISTER, LSB

**Address: 0x0B, Reset: 0x00, Name: YDATA_L**

[7:4] YDATA[3:0] (R)
Y-axis data.
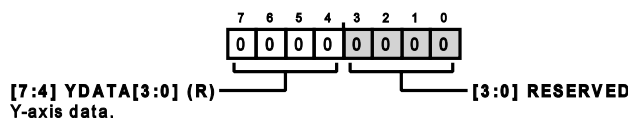
[3:0] RESERVED

*Table 25. Bit Descriptions for YDATA_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | YDATA[3:0] | | Y-axis data. | 0x0 | R |
| [3:0] | RESERVED | | Reserved. | 0x0 | R |

## REGISTER DETAILS

### Z-AXIS DATA REGISTER, MSB

**Address: 0x0C, Reset: 0x00, Name: ZDATA_H**

These two registers contain the z-axis acceleration data. Data is left justified and formatted as twos complement. ZDATA_H contains the eight MSBs, and ZDATA_L contains the four LSBs of the 12-bit value.
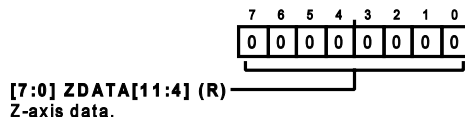


*Table 26. Bit Descriptions for ZDATA_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | ZDATA[11:4] | | Z-axis data. | 0x0 | R |

### Z-AXIS DATA REGISTER, LSB

**Address: 0x0D, Reset: 0x00, Name: ZDATA_L**
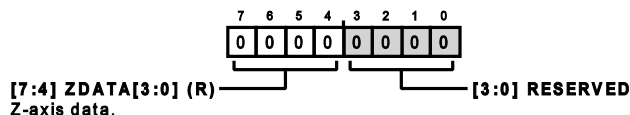


*Table 27. Bit Descriptions for ZDATA_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | ZDATA[3:0] | | Z-axis data. | 0x0 | R |
| [3:0] | RESERVED | | Reserved. | 0x0 | R |

### OFFSET TRIM REGISTERS

Offset trim registers are each four bits and offer user set, offset adjustments in twos complement format. The scale factor of these registers is shown in Figure 47.

### X-AXIS OFFSET TRIM REGISTER, LSB

**Address: 0x20, Reset: 0x00, Name: OFFSET_X**
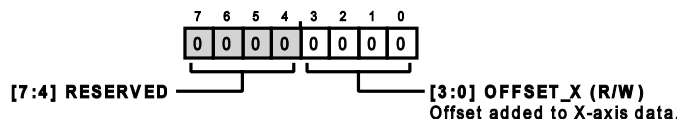


*Table 28. Bit Descriptions for OFFSET_X*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | RESERVED | | Reserved. | 0x0 | R |
| [3:0] | OFFSET_X | | Offset added to X-axis data. | 0x0 | R/W |

### Y-AXIS OFFSET TRIM REGISTER, LSB

**Address: 0x21, Reset: 0x00, Name: OFFSET_Y**
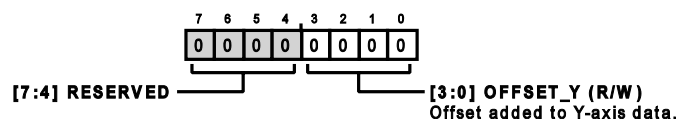
## REGISTER DETAILS

*Table 29. Bit Descriptions for OFFSET_Y*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | RESERVED | | Reserved. | 0x0 | R |
| [3:0] | OFFSET_Y | | Offset added to Y-axis data. | 0x0 | R/W |

## Z-AXIS OFFSET TRIM REGISTER, LSB

**Address: 0x22, Reset: 0x00, Name: OFFSET_Z**
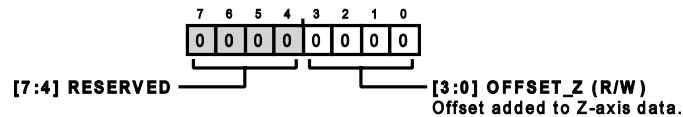


*Table 30. Bit Descriptions for OFFSET_Z*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:4] | RESERVED | | Reserved. | 0x0 | R |
| [3:0] | OFFSET_Z | | Offset added to Z-axis data. | 0x0 | R/W |

## X-AXIS ACTIVITY THRESHOLD REGISTER, MSB

**Address: 0x23, Reset: 0x00, Name: THRESH_ACT_X_H**

This 11-bit unsigned value sets the threshold for activity detection. This value is set in codes and the scale factor is 100 m$g$ per code. To detect activity, the absolute value of the 12-bit acceleration data is compared with the 11-bit (unsigned) activity threshold value. The THRESH_ACT_X_L register contains the least significant bits, and the THRESH_ACT_X_H register contains the most significant byte of the activity threshold value.



*Table 31. Bit Descriptions for THRESH_ACT_X_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_ACT_X[10:3] | | Threshold for activity detection. The 8 MSBs of x-axis threshold. | 0x0 | R/W |

## X-AXIS OF ACTIVITY THRESHOLD REGISTER, LSB

**Address: 0x24, Reset: 0x00, Name: THRESH_ACT_X_L**



*Table 32. Bit Descriptions for THRESH_ACT_X_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:5] | THRESH_ACT_X[2:0] | | Threshold for activity detection. The 3 LSBs of x-axis threshold. | 0x0 | R/W |

## REGISTER DETAILS

*Table 32. Bit Descriptions for THRESH_ACT_X_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [4:2] | RESERVED | | Reserved. | 0x0 | R |
| 1 | ACT_REF | | Selects referenced or absolute activity processing. | 0x0 | R/W |
| | | 1 | Referenced activity processing. | | |
| | | 0 | Absolute activity processing. | | |
| 0 | ACT_X_EN | | Enable activity detection using X-axis data. | 0x0 | R/W |
| | | 0 | X-axis ignored. | | |
| | | 1 | X-axis used. | | |

## Y-AXIS ACTIVITY THRESHOLD REGISTER, MSB

**Address: 0x25, Reset: 0x00, Name: THRESH_ACT_Y_H**



[7:0] THRESH_ACT_Y[10:3] (R/W)
Threshold for activity detection.
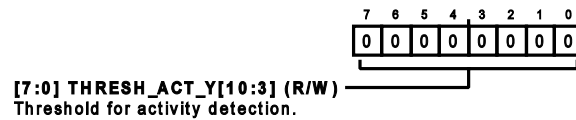
*Table 33. Bit Descriptions for THRESH_ACT_Y_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_ACT_Y[10:3] | | Threshold for activity detection. The 8 MSBs of y-axis threshold. | 0x0 | R/W |

## Y-AXIS OF ACTIVITY THRESHOLD REGISTER, LSB

**Address: 0x26, Reset: 0x00, Name: THRESH_ACT_Y_L**



[7:5] THRESH_ACT_Y[2:0] (R/W)
Threshold for activity detection.

[4:1] RESERVED

[0] ACT_Y_EN (R/W)
Enable activity detection using Y-axis data.
0:  Y-axis ignored.
1:  Y-axis used.

*Table 34. Bit Descriptions for THRESH_ACT_Y_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:5] | THRESH_ACT_Y[2:0] | | Threshold for activity detection. The 3 LSBs of y-axis threshold. | 0x0 | R/W |
| [4:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | ACT_Y_EN | | Enable activity detection using Y-axis data. | 0x0 | R/W |
| | | 0 | Y-axis ignored. | | |
| | | 1 | Y-axis used. | | |

## Z-AXIS ACTIVITY THRESHOLD REGISTER, MSB

**Address: 0x27, Reset: 0x00, Name: THRESH_ACT_Z_H**



[7:0] THRESH_ACT_Z[10:3] (R/W)
Threshold for activity detection.
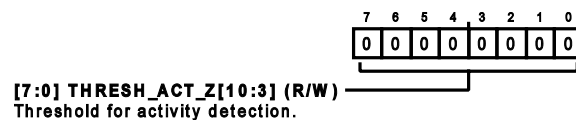
*Table 35. Bit Descriptions for THRESH_ACT_Z_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_ACT_Z[10:3] | | Threshold for activity detection. The 8 MSBs of z-axis threshold. | 0x0 | R/W |

## REGISTER DETAILS

### Z-AXIS OF ACTIVITY THRESHOLD REGISTER, LSB

**Address: 0x28, Reset: 0x00, Name: THRESH_ACT_Z_L**

```
        7  6  5  4  3  2  1  0
       ┌──┬──┬──┬──┬──┬──┬──┬──┐
       │0 │0 │0 │0 │0 │0 │0 │0 │
       └──┴──┴──┴──┴──┴──┴──┴──┘
```

[7:5] THRESH_ACT_Z[2:0] (R/W)
Threshold for activity detection.

[4:1] RESERVED

[0] ACT_Z_EN (R/W)
Enable activity detection using Z-axis data.
  0:  Z-axis ignored.
  1:  Z-axis used.
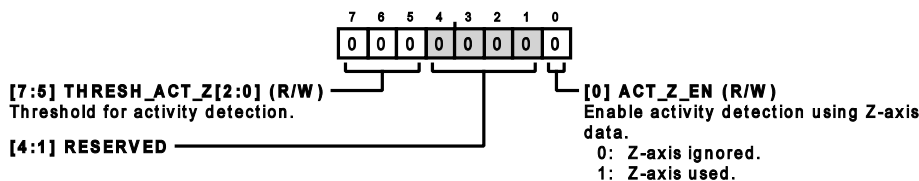
*Table 36. Bit Descriptions for THRESH_ACT_Z_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:5] | THRESH_ACT_Z[2:0] | | Threshold for activity detection. The 3 LSBs of z-axis threshold. | 0x0 | R/W |
| [4:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | ACT_Z_EN | | Enable activity detection using Z-axis data. | 0x0 | R/W |
| | | 0 | Z-axis ignored. | | |
| | | 1 | Z-axis used. | | |

### ACTIVITY TIME REGISTER

**Address: 0x29, Reset: 0x00, Name: TIME_ACT**

The activity timer implements a robust activity detection that minimizes false positive motion triggers. When the timer is used, only sustained motion can trigger activity detection. The time (in milliseconds) is given by the following equation:

$Time = TIME\_ACT \times 4.125$ ms per code

where:
$TIME\_ACT$ is the value set in this register.
4.125 ms per code is the scale factor of the TIME_ACT register for ODR = 5120 Hz. It is 8.25 ms per code for ODR = 2560 Hz and lower. See the Activity Timer section for more information.

```
        7  6  5  4  3  2  1  0
       ┌──┬──┬──┬──┬──┬──┬──┬──┐
       │0 │0 │0 │0 │0 │0 │0 │0 │
       └──┴──┴──┴──┴──┴──┴──┴──┘
```

[7:0] ACT_COUNT (R/W)
Number of multiples of 4.125 ms activity timer for which above threshold acceleration is required to detect activity.
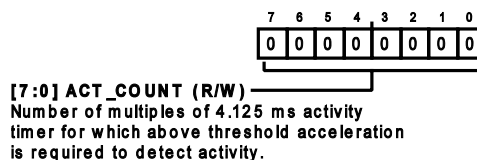
*Table 37. Bit Descriptions for TIME_ACT*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | ACT_COUNT | | Number of multiples of 4.125 ms activity timer for which above threshold acceleration is required to detect activity. It is 4.125 ms per code for 5120 Hz ODR, and it is 8.25 ms per code for 2560 Hz ODR and lower. | 0x0 | R/W |

### X-AXIS INACTIVITY THRESHOLD REGISTER, MSB

**Address: 0x2A, Reset: 0x00, Name: THRESH_INACT_X_H**

This 11-bit unsigned value sets the threshold for inactivity detection. This value is set in codes, and the scale factor is 100 m*g* per code. To detect inactivity, the absolute value of the 12-bit acceleration data is compared with the 11-bit (unsigned) inactivity threshold value. The THRESH_INACT_X_L register contains the least significant bits, and the THRESH_INACT_X_H register contains the most significant byte of the inactivity threshold value.

```
        7  6  5  4  3  2  1  0
       ┌──┬──┬──┬──┬──┬──┬──┬──┐
       │0 │0 │0 │0 │0 │0 │0 │0 │
       └──┴──┴──┴──┴──┴──┴──┴──┘
```

[7:0] THRESH_INACT_X[10:3] (R/W)
Threshold for inactivity detection.

## REGISTER DETAILS

*Table 38. Bit Descriptions for THRESH_INACT_X_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_INACT_X[10:3] | | Threshold for inactivity detection. The 8 MSBs of x-axis. | 0x0 | R/W |

## X-AXIS OF INACTIVITY THRESHOLD REGISTER, LSB

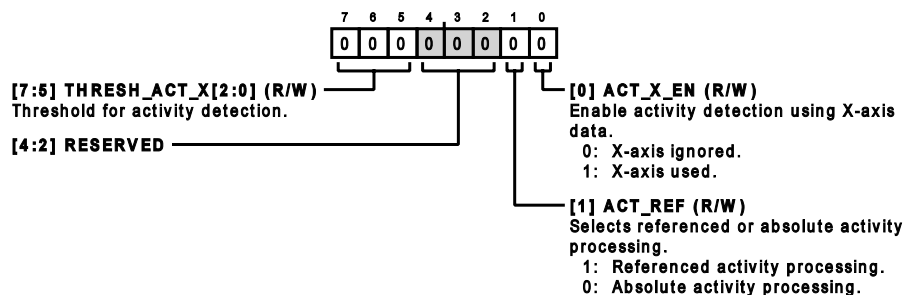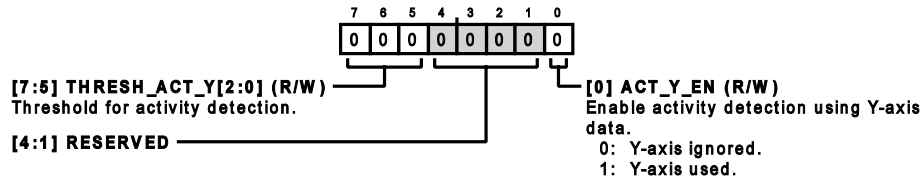**Address: 0x2B, Reset: 0x00, Name: THRESH_INACT_X_L**
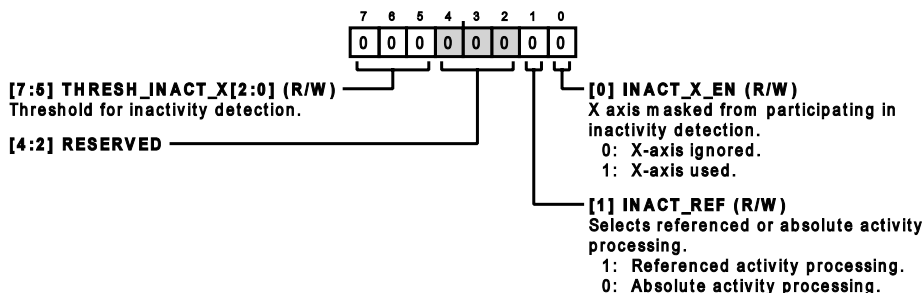


*Table 39. Bit Descriptions for THRESH_INACT_X_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:5] | THRESH_INACT_X[2:0] | | Threshold for inactivity detection. The 3 LSBs of the x-axis. | 0x0 | R/W |
| [4:2] | RESERVED | | Reserved. | 0x0 | R |
| 1 | INACT_REF | | Selects referenced or absolute inactivity processing. | 0x0 | R/W |
| | | 1 | Referenced inactivity processing. | | |
| | | 0 | Absolute inactivity processing. | | |
| 0 | INACT_X_EN | | X-axis masked from participating in inactivity detection. | 0x0 | R/W |
| | | 0 | X-axis ignored. | | |
| | | 1 | X-axis used. | | |

## Y-AXIS INACTIVITY THRESHOLD REGISTER, MSB

**Address: 0x2C, Reset: 0x00, Name: THRESH_INACT_Y_H**



*Table 40. Bit Descriptions for THRESH_INACT_Y_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_INACT_Y[10:3] | | Threshold for inactivity detection. The 8 MSBs of the y-axis. | 0x0 | R/W |

## Y-AXIS OF INACTIVITY THRESHOLD REGISTER, LSB

**Address: 0x2D, Reset: 0x00, Name: THRESH_INACT_Y_L**
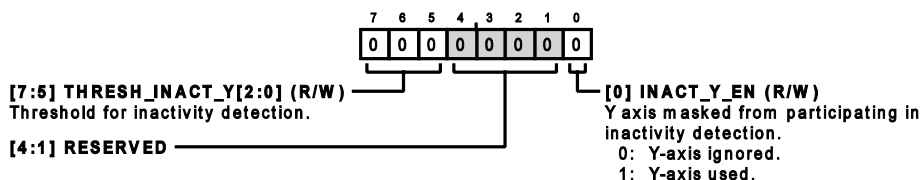
## REGISTER DETAILS

*Table 41. Bit Descriptions for THRESH_INACT_Y_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:5] | THRESH_INACT_Y[2:0] | | Threshold for inactivity detection. The 3 LSBs of the y-axis. | 0x0 | R/W |
| [4:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | INACT_Y_EN | | Y-axis masked from participating in inactivity detection. | 0x0 | R/W |
| | | 0 | Y-axis ignored. | | |
| | | 1 | Y-axis used. | | |

## Z-AXIS INACTIVITY THRESHOLD REGISTER, MSB

**Address: 0x2E, Reset: 0x00, Name: THRESH_INACT_Z_H**



[7:0] THRESH_INACT_Z[10:3] (R/W)
Threshold for inactivity detection.
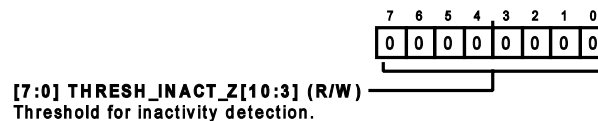
*Table 42. Bit Descriptions for THRESH_INACT_Z_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_INACT_Z[10:3] | | Threshold for inactivity detection. The 8 MSBs of the z-axis. | 0x0 | R/W |

## Z-AXIS OF INACTIVITY THRESHOLD REGISTER, LSB

**Address: 0x2F, Reset: 0x00, Name: THRESH_INACT_Z_L**



[7:5] THRESH_INACT_Z[2:0] (R/W)
Threshold for inactivity detection.

[4:1] RESERVED

[0] INACT_Z_EN (R/W)
Z axis masked from participating in inactivity detection.
0: Z-axis ignored.
1: Z-axis used.
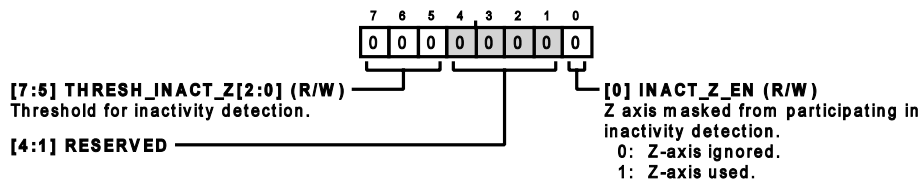
*Table 43. Bit Descriptions for THRESH_INACT_Z_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:5] | THRESH_INACT_Z[2:0] | | Threshold for inactivity detection. The 3 LSBs of the z-axis. | 0x0 | R/W |
| [4:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | INACT_Z_EN | | Z-axis masked from participating in inactivity detection. | 0x0 | R/W |
| | | 0 | Z-axis ignored. | | |
| | | 1 | Z-axis used. | | |

## INACTIVITY TIME REGISTERS

The 16-bit value in these registers sets the time that all enabled axes must be lower than the inactivity threshold for an inactivity event to be detected. The TIME_INACT_L register holds the eight LSBs, and the TIME_INACT_H register holds the eight MSBs of the 16-bit TIME_INACT value.

Calculate the time as follows:

*Time = TIME_INACT* × 32.5 ms per code

where:
*TIME_INACT* is the 16-bit value set by the TIME_INACT_L register (eight LSBs) and the TIME_INACT_H register (eight MSBs).
32.5 ms per code is the scale factor of the TIME_INACT_L and TIME_INACT_H registers for 2560 Hz and lower. It is 16.25 ms per code of ODR = 5120 Hz. See the Inactivity Timer section for more information.

## REGISTER DETAILS

### INACTIVITY TIMER REGISTER, MSB

**Address: 0x30, Reset: 0x00, Name: TIME_INACT_H**
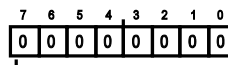
```
         7  6  5  4  3  2  1  0
        ┌──┬──┬──┬──┬──┬──┬──┬──┐
        │0 │0 │0 │0 │0 │0 │0 │0 │
        └──┴──┴──┴──┴──┴──┴──┴──┘
[7:0] INACT_COUNT[15:8] (R/W)
Number of multiples of 32.5 ms inactivity
timer below which the threshold acceleration
is required to detect inactivity
```

*Table 44. Bit Descriptions for TIME_INACT_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | INACT_COUNT[15:8] | | Number of multiples of 32.5 ms inactivity timer below which the threshold acceleration is required to detect inactivity. It is 32.5 ms per code for 2560 Hz ODR and lower, and it is 16.25 ms per code for 5120 Hz ODR. | 0x0 | R/W |

### INACTIVITY TIMER REGISTER, LSB

**Address: 0x31, Reset: 0x00, Name: TIME_INACT_L**
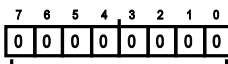
```
         7  6  5  4  3  2  1  0
        ┌──┬──┬──┬──┬──┬──┬──┬──┐
        │0 │0 │0 │0 │0 │0 │0 │0 │
        └──┴──┴──┴──┴──┴──┴──┴──┘
[7:0] INACT_COUNT[7:0] (R/W)
Number of multiples of 32.5 ms inactivity
timer below which the threshold acceleration
is required to detect inactivity
```

*Table 45. Bit Descriptions for TIME_INACT_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | INACT_COUNT[7:0] | | Number of multiples of 32.5 ms inactivity timer below which the threshold acceleration is required to detect inactivity. | 0x0 | R/W |

### X-AXIS MOTION WARNING THRESHOLD REGISTER, MSB

**Address: 0x32, Reset: 0x00, Name: THRESH_ACT2_X_H**

This 11-bit unsigned value sets the threshold for motion detection. This value is set in codes, and the scale factor is 100 m$g$ per code. To detect motion, the absolute value of the 12-bit acceleration data is compared with the 11-bit (unsigned) ACTIVITY2 threshold value. The THRESH_ACT2_X_L register contains the least significant bits, and the THRESH_ACT2_X_H register contains the most significant byte of the ACTIVITY2 threshold value.
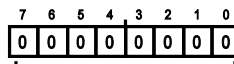
```
         7  6  5  4  3  2  1  0
        ┌──┬──┬──┬──┬──┬──┬──┬──┐
        │0 │0 │0 │0 │0 │0 │0 │0 │
        └──┴──┴──┴──┴──┴──┴──┴──┘
[7:0] THRESH_ACT2_X[10:3] (R/W)
OTN Threshold.
```

*Table 46. Bit Descriptions for THRESH_ACT2_X_H*

| Bits | Bit Name | Settings | Description[1] | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_ACT2_X[10:3] | | OTN Threshold. The 8 MSBs of the x-axis threshold for motion warning interrupt. | 0x0 | R/W |

[1] OTN stands for other threshold notification.

### X-AXIS OF MOTION WARNING NOTIFICATION REGISTER, LSB

**Address: 0x33, Reset: 0x00, Name: THRESH_ACT2_X_L**

## REGISTER DETAILS
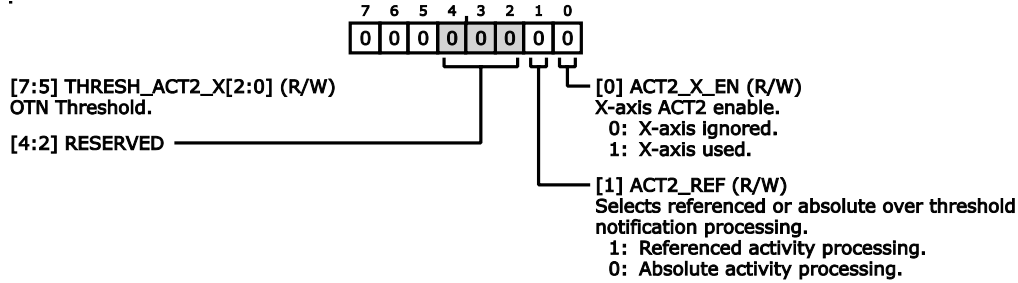


*Table 47. Bit Descriptions for THRESH_ACT2_X_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | THRESH_ACT2_X[2:0] | | OTN Threshold. The 3 LSBs of the x-axis threshold for motion warning interrupt. | 0x0 | R/W |
| [4:2] | RESERVED | | Reserved. | 0x0 | R |
| 1 | ACT2_REF | | Selects referenced or absolute over threshold notification processing. | 0x0 | R/W |
| | | 1 | Referenced activity processing. | | |
| | | 0 | Absolute activity processing. | | |
| 0 | ACT2_X_EN | | X-axis ACT2 enable. When set to 1, the x-axis participates in motion warning notification detection. | 0x0 | R/W |
| | | 0 | X-axis ignored. | | |
| | | 1 | X-axis used. | | |

## Y-AXIS MOTION WARNING NOTIFICATION THRESHOLD REGISTER, MSB

**Address: 0x34, Reset: 0x00, Name: THRESH_ACT2_Y_H**
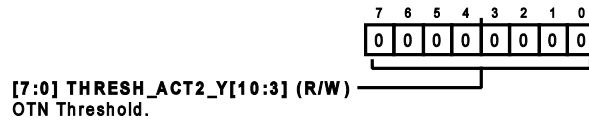


*Table 48. Bit Descriptions for THRESH_ACT2_Y_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | THRESH_ACT2_Y[10:3] | | OTN Threshold. The 8 MSBs of the y-axis threshold for motion warning interrupt. | 0x0 | R/W |

## Y-AXIS OF MOTION WARNING NOTIFICATION REGISTER, LSB

**Address: 0x35, Reset: 0x00, Name: THRESH_ACT2_Y_L**



*Table 49. Bit Descriptions for THRESH_ACT2_Y_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | THRESH_ACT2_Y[2:0] | | OTN Threshold. The 3 LSBs of the y-axis threshold for motion warning interrupt. | 0x0 | R/W |
| [4:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | ACT2_Y_EN | | Y-axis ACT2 enable. When 1, the y-axis participates in motion warning notification detection. | 0x0 | R/W |
| | | 0 | Y-axis ignored. | | |
| | | 1 | Y-axis used. | | |

## REGISTER DETAILS

### Z-AXIS MOTION WARNING NOTIFICATION THRESHOLD REGISTER, MSB

**Address: 0x36, Reset: 0x00, Name: THRESH_ACT2_Z_H**

```
        7 6 5 4 3 2 1 0
       ┌─┬─┬─┬─┬─┬─┬─┬─┐
       │0│0│0│0│0│0│0│0│
       └─┴─┴─┴─┴─┴─┴─┴─┘
[7:0] THRESH_ACT2_Z[10:3] (R/W)
OTN Threshold.
```

*Table 50. Bit Descriptions for THRESH_ACT2_Z_H*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:0] | THRESH_ACT2_Z[10:3] | | OTN Threshold. The 8 MSBs of the z-axis threshold for motion warning interrupt. | 0x0 | R/W |

### Z-AXIS MOTION WARNING NOTIFICATION REGISTER, LSB

**Address: 0x37, Reset: 0x00, Name: THRESH_ACT2_Z_L**

```
        7 6 5 4 3 2 1 0
       ┌─┬─┬─┬─┬─┬─┬─┬─┐
       │0│0│0│0│0│0│0│0│
       └─┴─┴─┴─┴─┴─┴─┴─┘
[7:5] THRESH_ACT2_Z[2:0] (R/W)       [0] ACT2_Z_EN (R/W)
OTN Threshold.                        Z axis ACT2 enable.
                                        0:  Z-axis ignored.
[4:1] RESERVED                          1:  Z-axis used.
```
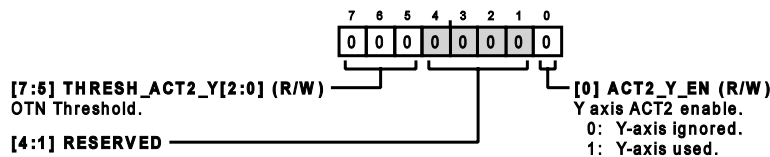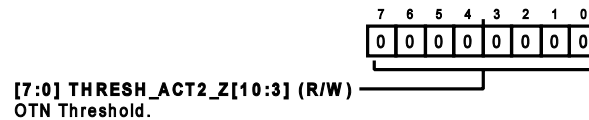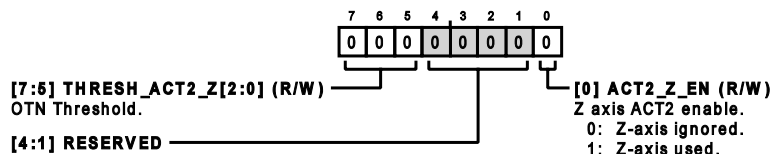
*Table 51. Bit Descriptions for THRESH_ACT2_Z_L*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:5] | THRESH_ACT2_Z[2:0] | | OTN Threshold. The 3 LSBs of the z-axis threshold for motion warning interrupt. | 0x0 | R/W |
| [4:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | ACT2_Z_EN | | Z-axis ACT2 enable. When 1, the z-axis participates in motion warning notification detection. | 0x0 | R/W |
| | | 0 | Z-axis ignored. | | |
| | | 1 | Z-axis used. | | |

### HIGH-PASS FILTER SETTINGS REGISTER

**Address: 0x38, Reset: 0x00, Name: HPF**

Use this register to specify parameters for the internal high-pass filter.

```
        7 6 5 4 3 2 1 0
       ┌─┬─┬─┬─┬─┬─┬─┬─┐
       │0│0│0│0│0│0│0│0│
       └─┴─┴─┴─┴─┴─┴─┴─┘
[7:2] RESERVED              [1:0] HPF_CORNER (R/W)
                            High-Pass Filter Corner Frequency Selection
                               00:  High Pass Filter Corner 0.
                               01:  High Pass Filter Corner 1.
                               10:  High Pass Filter Corner 2.
                               11:  High Pass Filter Corner 3.
```

*Table 52. Bit Descriptions for HPF*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| [7:2] | RESERVED | | Reserved. | 0x0 | R |
| [1:0] | HPF_CORNER | | High-Pass Filter Corner Frequency Selection. | 0x0 | R/W |
| | | 00 | High-Pass Filter Corner 0. At ODR 5120 Hz = 30.48 Hz, at ODR 2560 Hz = 15.24 Hz, at ODR 1280 Hz = 7.61 Hz, at ODR 640 Hz = 3.81 Hz, and at ODR 320 Hz = 1.90 Hz. | | |
| | | 01 | High-Pass Filter Corner 1. At ODR 5120 Hz = 15.58 Hz, at ODR 2560 Hz = 7.79 Hz, at ODR 1280 Hz = 3.89 Hz, at ODR 640 Hz = 1.94 Hz, and at ODR 320 Hz = 0.97 Hz. | | |
| | | 10 | High-Pass Filter Corner 2. At ODR 5120 Hz = 7.88 Hz, at ODR 2560 Hz = 3.94 Hz, at ODR 1280 Hz = 1.97 Hz, at ODR 640 Hz = 0.98 Hz, and at ODR 320 Hz = 0.49 Hz. | | |

## REGISTER DETAILS

*Table 52. Bit Descriptions for HPF*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| | | 11 | High-Pass Filter Corner 3. At ODR 5120 Hz = 3.96 Hz, at ODR 2560 Hz = 1.98 Hz, at ODR 1280 Hz = 0.99 Hz, at ODR 640 Hz = 0.49 Hz, and at ODR 320 Hz = 0.24 Hz. | | |

## FIFO SAMPLES REGISTER

**Address: 0x39, Reset: 0x80, Name: FIFO_SAMPLES**

Use the FIFO_SAMPLES value to specify the number of samples to store in the FIFO. The 8 least significant bits (LSBs) of the FIFO_SAMPLES value are stored in this register. The most significant bit (MSB) of the FIFO_SAMPLES value is Bit 0 of the FIFO_CTL register.

The default value of this register is 0x80 to avoid triggering the FIFO watermark interrupt (see the FIFO Watermark section for more information). In trigger FIFO mode, FIFO_SAMPLES program the number of samples to be saved after the trigger is detected.

```
 7  6  5  4  3  2  1  0
 1  0  0  0  0  0  0  0
```
[7:0] FIFO_SAMPLES[7:0] (R/W)
FIFO Samples.
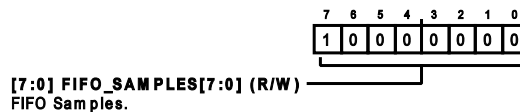
*Table 53. Bit Descriptions for FIFO_SAMPLES*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | FIFO_SAMPLES[7:0] | | FIFO Samples. Watermark number of FIFO samples that triggers a FIFO_FULL condition when reached. Values range from 0 to 512. | 0x80 | R/W |

## FIFO CONTROL REGISTER

**Address: 0x3A, Reset: 0x00, Name: FIFO_CTL**

Use this register to specify the operating parameters for the FIFO.

```
 7  6  5  4  3  2  1  0
 0  0  0  0  0  0  0  0
```
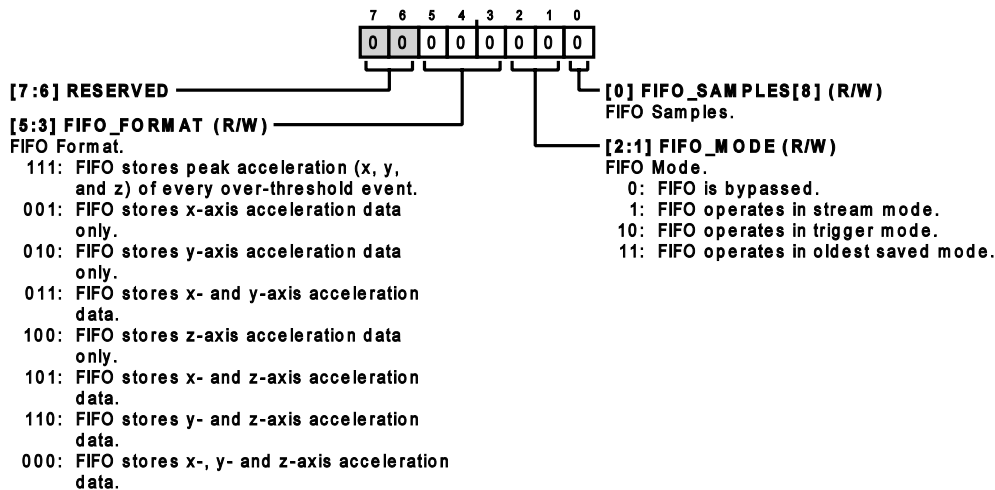[7:6] RESERVED
[5:3] FIFO_FORMAT (R/W)
FIFO Format.
  111: FIFO stores peak acceleration (x, y, and z) of every over-threshold event.
  001: FIFO stores x-axis acceleration data only.
  010: FIFO stores y-axis acceleration data only.
  011: FIFO stores x- and y-axis acceleration data.
  100: FIFO stores z-axis acceleration data only.
  101: FIFO stores x- and z-axis acceleration data.
  110: FIFO stores y- and z-axis acceleration data.
  000: FIFO stores x-, y- and z-axis acceleration data.

[0] FIFO_SAMPLES[8] (R/W)
FIFO Samples.
[2:1] FIFO_MODE (R/W)
FIFO Mode.
  0: FIFO is bypassed.
  1: FIFO operates in stream mode.
  10: FIFO operates in trigger mode.
  11: FIFO operates in oldest saved mode.

*Table 54. Bit Descriptions for FIFO_CTL*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:6] | RESERVED | | Reserved. | 0x0 | R |
| [5:3] | FIFO_FORMAT | | FIFO Format. Specifies which data is stored in the FIFO buffer. | 0x0 | R/W |
| | | 111 | FIFO stores peak acceleration (x, y, and z) of every over threshold event. | | |
| | | 001 | FIFO stores x-axis acceleration data only. | | |
| | | 010 | FIFO stores y-axis acceleration data only. | | |

## REGISTER DETAILS

*Table 54. Bit Descriptions for FIFO_CTL*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| | | 011 | FIFO stores x- and y-axis acceleration data. | | |
| | | 100 | FIFO stores z-axis acceleration data only. | | |
| | | 101 | FIFO stores x- and z-axis acceleration data. | | |
| | | 110 | FIFO stores y- and z-axis acceleration data. | | |
| | | 000 | FIFO stores x-, y- and z-axis acceleration data. | | |
| [2:1] | FIFO_MODE | | FIFO Mode. Specifies FIFO operating mode. | 0x0 | R/W |
| | | 0 | FIFO is bypassed. | | |
| | | 1 | FIFO operates in stream mode. | | |
| | | 10 | FIFO operates in trigger mode. | | |
| | | 11 | FIFO operates in oldest saved mode. | | |
| 0 | FIFO_SAMPLES[8] | | FIFO Samples. Watermark number of FIFO samples that triggers a FIFO_FULL condition when reached. Values range from 0 to 512. | 0x0 | R/W |

## INTERRUPT PIN FUNCTION MAP REGISTERS

### Address: 0x3B, Reset: 0x00, Name: INT1_MAP

The INT1_MAP and INT2_MAP registers configure the INT1 and INT2 interrupt pins, respectively. Bits[6:0] select which function(s) generate an interrupt on the pin. If its corresponding bit is set to 1, the function generates an interrupt on the INTx pin. Bit B7 configures whether the pin operates in active high (B7 low) or active low (B7 high) mode. Any number of functions can be selected simultaneously for each pin. If multiple functions are selected, their conditions are OR'ed together to determine the INTx pin state. The status of each function can be determined by reading the status register. If no interrupts are mapped to an INTx pin, the pin remains in a high impedance state.
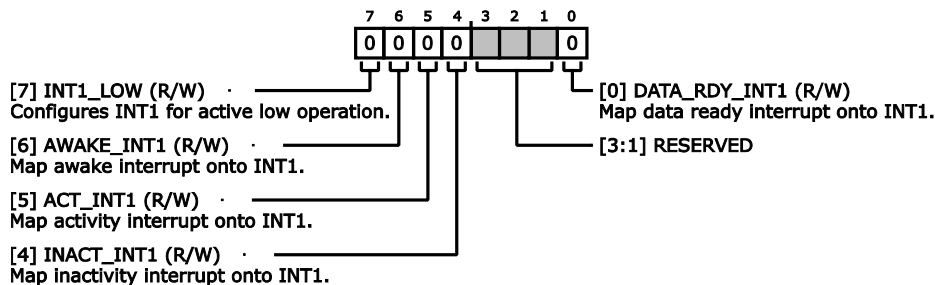


*Table 55. Bit Descriptions for INT1_MAP*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | INT1_LOW | | Configures INT1 for active low operation. | 0x0 | R/W |
| 6 | AWAKE_INT1 | | Map awake interrupt onto INT1. | 0x0 | R/W |
| 5 | ACT_INT1 | | Map activity interrupt onto INT1. | 0x0 | R/W |
| 4 | INACT_INT1 | | Map inactivity interrupt onto INT1. | 0x0 | R/W |
| [3:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | DATA_RDY_INT1 | | Map data ready interrupt onto INT1. | 0x0 | R/W |

## INT2 FUNCTION MAP REGISTER

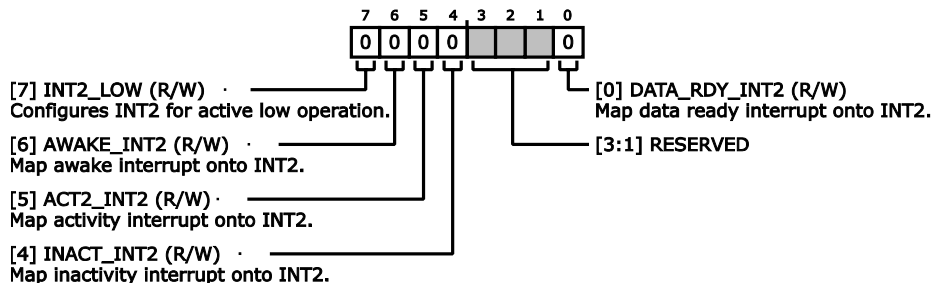### Address: 0x3C, Reset: 0x00, Name: INT2_MAP

## REGISTER DETAILS



[7] INT2_LOW (R/W)
Configures INT2 for active low operation.

[6] AWAKE_INT2 (R/W)
Map awake interrupt onto INT2.

[5] ACT2_INT2 (R/W)
Map activity interrupt onto INT2.

[4] INACT_INT2 (R/W)
Map inactivity interrupt onto INT2.

[0] DATA_RDY_INT2 (R/W)
Map data ready interrupt onto INT2.

[3:1] RESERVED

*Table 56. Bit Descriptions for INT2_MAP*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | INT2_LOW | | Configures INT2 for active low operation. | 0x0 | R/W |
| 6 | AWAKE_INT2 | | Map awake interrupt onto INT2. | 0x0 | R/W |
| 5 | ACT2_INT2 | | Map activity interrupt onto INT2. | 0x0 | R/W |
| 4 | INACT_INT2 | | Map inactivity interrupt onto INT2. | 0x0 | R/W |
| [3:1] | RESERVED | | Reserved. | 0x0 | R |
| 0 | DATA_RDY_INT2 | | Map data ready interrupt onto INT2. | 0x0 | R/W |

## EXTERNAL TIMING CONTROL REGISTER

### Address: 0x3D, Reset: 0x00, Name: TIMING

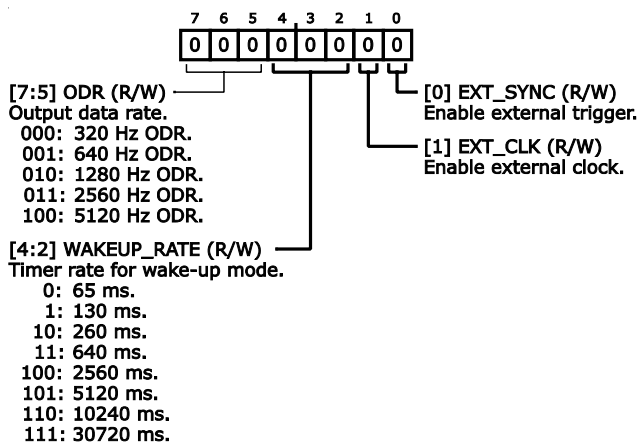Use this register to control the ADXL371 timing parameters: ODR and external timing triggers.



[7:5] ODR (R/W)
Output data rate.
  000: 320 Hz ODR.
  001: 640 Hz ODR.
  010: 1280 Hz ODR.
  011: 2560 Hz ODR.
  100: 5120 Hz ODR.

[4:2] WAKEUP_RATE (R/W)
Timer rate for wake-up mode.
  0: 65 ms.
  1: 130 ms.
  10: 260 ms.
  11: 640 ms.
  100: 2560 ms.
  101: 5120 ms.
  110: 10240 ms.
  111: 30720 ms.

[0] EXT_SYNC (R/W)
Enable external trigger.

[1] EXT_CLK (R/W)
Enable external clock.

*Table 57. Bit Descriptions for TIMING*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:5] | ODR | | Output data rate. | 0x0 | R/W |
| | | 000 | 320 Hz ODR. | | |
| | | 001 | 640 Hz ODR. | | |
| | | 010 | 1280 Hz ODR. | | |
| | | 011 | 2560 Hz ODR. | | |
| | | 100 | 5120 Hz ODR. | | |
| [4:2] | WAKEUP_RATE | | Timer rate for wake-up mode. | 0x0 | R/W |
| | | 0 | 65 ms. | | |
| | | 1 | 130 ms. | | |

## REGISTER DETAILS

*Table 57. Bit Descriptions for TIMING*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| | | 10 | 260 ms. | | |
| | | 11 | 640 ms. | | |
| | | 100 | 2560 ms. | | |
| | | 101 | 5120 ms. | | |
| | | 110 | 10240 ms. | | |
| | | 111 | 30720 ms. | | |
| 1 | EXT_CLK | | Enable external clock. | 0x0 | R/W |
| 0 | EXT_SYNC | | Enable external trigger. | 0x0 | R/W |

## MEASUREMENT CONTROL REGISTER

**Address: 0x3E, Reset: 0x00, Name: MEASURE**

Use this register to control several measurement settings.



*Table 58. Bit Descriptions for MEASURE*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | USER_OR_DISABLE | | User overrange disable. | 0x0 | R/W |
| 6 | AUTOSLEEP | | Autosleep. When set to 1, autosleep is enabled, and the device enters wake-up mode automatically upon detection of inactivity. Activity and inactivity detection must be in linked mode or loop mode (the LINKLOOP bits in the MEASURE register) to enable autosleep. Otherwise, the bit is ignored. | 0x0 | R/W |
| [5:4] | LINKLOOP | | Link/loop activity processing. These bits select how activity and inactivity processing are linked. | 0x0 | R/W |
| | | 0 | Default mode. Activity and inactivity detection, when enabled, operate simultaneously and their interrupts (if mapped) must be acknowledged by the host processor by reading the STATUS register. Autosleep is disabled in this mode. | | |
| | | 1 | Linked mode. Activity and inactivity detection are linked sequentially so that only one is enabled at a time. Their interrupts (if mapped) must be acknowledged by the host processor by reading the STATUS register. | | |
| | | 10 | Looped mode. Activity and inactivity detection are linked sequentially so that only one is enabled at a time, and their interrupts are internally acknowledged (do not need to be serviced by the host processor). To use either linked or looped mode, both ACT_x_EN and INACT_x_EN must be set to 1. Otherwise, the default mode is used. For additional information, refer to the Linking Activity and Inactivity Detection section. | | |
| 3 | LOW_NOISE | | Low noise. Selects low noise operation. | 0x0 | R/W |
| | | 0 | Normal operation. Device operates at the normal noise level and ultralow current consumption | | |
| | | 1 | Low noise operation. Device operates at ~1/3 the normal noise level. | | |
| [2:0] | BANDWIDTH | | Bandwidth. Select the desired output signal bandwidth. A four-pole low-pass filter at the selected frequency limits the signal bandwidth. | 0x0 | R/W |
| | | 000 | 160 Hz bandwidth. | | |
| | | 001 | 320 Hz bandwidth. | | |

## REGISTER DETAILS

*Table 58. Bit Descriptions for MEASURE*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
|  |  | 010 | 640 Hz bandwidth. |  |  |
|  |  | 011 | 1280 Hz bandwidth. |  |  |
|  |  | 100 | 2560 Hz bandwidth. |  |  |

## POWER CONTROL REGISTER

**Address: 0x3F, Reset: 0x00, Name: POWER_CTL**
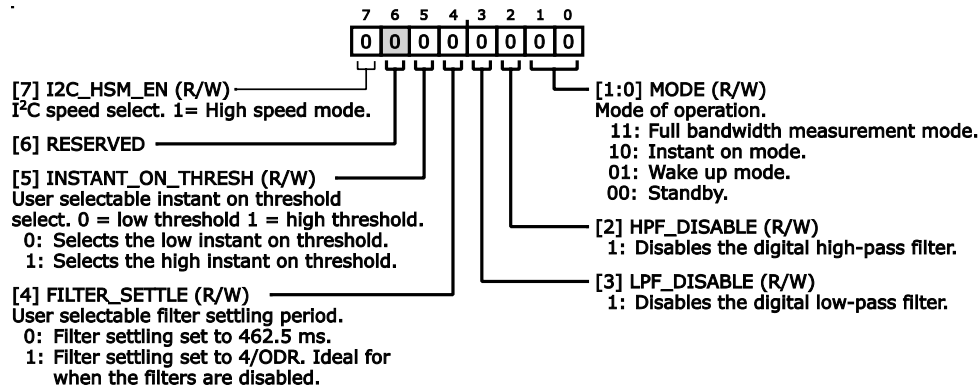


*Table 59. Bit Descriptions for POWER_CTL*

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7 | I2C_HSM_EN |  | I²C speed select. 1 = High speed mode. | 0x0 | R/W |
| 6 | RESERVED |  | Reserved. | 0x0 | R |
| 5 | INSTANT_ON_THRESH |  | User selectable instant on threshold select. 0 = low threshold, 1 = high threshold. | 0x0 | R/W |
|  |  | 0 | Selects the low instant on threshold. |  |  |
|  |  | 1 | Selects the high instant on threshold. |  |  |
| 4 | FILTER_SETTLE |  | User selectable filter settling period. | 0x0 | R/W |
|  |  | 0 | Filter settling set to 462.5 ms. |  |  |
|  |  | 1 | Filter settling set to 4/ODR. Ideal for when the filters are disabled. |  |  |
| 3 | LPF_DISABLE | 1 | Disables the low-pass filter. | 0x0 | R/W |
| 2 | HPF_DISABLE | 1 | Disables the digital high-pass filter. | 0x0 | R/W |
| [1:0] | MODE |  | Mode of operation. | 0x0 | R/W |
|  |  | 11 | Full bandwidth measurement mode. |  |  |
|  |  | 10 | Instant on mode. |  |  |
|  |  | 01 | Wake up mode. |  |  |
|  |  | 00 | Standby. |  |  |

## SELF TEST REGISTER

**Address: 0x40, Reset: 0x00, Name: SELF_TEST**

Refer to the Self Test section for information on the operation of the self test feature, and see the Self Test Procedure section for guidelines on how to use this functionality.
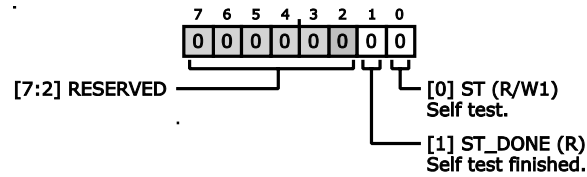
## REGISTER DETAILS



*Table 60. Bit Descriptions for SELF_TEST*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:2] | RESERVED | | Reserved. | 0x0 | R |
| 1 | ST_DONE | | Self test finished. | 0x0 | R |
| 0 | ST | | Self test. Writing a 1 to this bit initiates self test. Writing a 0 clears self test. | 0x0 | R/W |

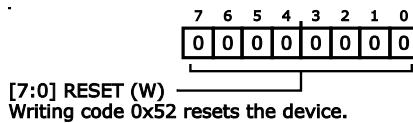## RESET (CLEARS) REGISTER, PART IN STANDBY MODE

**Address: 0x41, Reset: 0x00, Name: RESET**



*Table 61. Bit Descriptions for RESET*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | RESET | | Writing code 0x52 resets the device. | 0x0 | W |

## FIFO ACCESS REGISTER

**Address: 0x42, Reset: 0x00, Name: FIFO_DATA**

Read this register to access data stored in the FIFO.
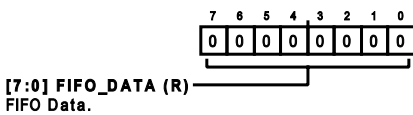


*Table 62. Bit Descriptions for FIFO_DATA*

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | FIFO_DATA | | FIFO Data. A read to this address pops a 2-byte word of axis data from the FIFO. FIFO data is formatted to 2 bytes (16 bits), most significant byte first. Two subsequent reads complete the transaction of this data onto the interface. Continued reading of this field continues to pop the FIFO every third read. Multibyte reads to this address do not increment the address pointer. If this address is read due to an auto-increment from the previous address, it does not pop the FIFO. It returns zeros and increment on to the next address. | 0x0 | R |

## APPLICATIONS INFORMATION

### APPLICATION EXAMPLES

This section includes application circuits highlighting useful features of the ADXL371.

### Power Supply Decoupling

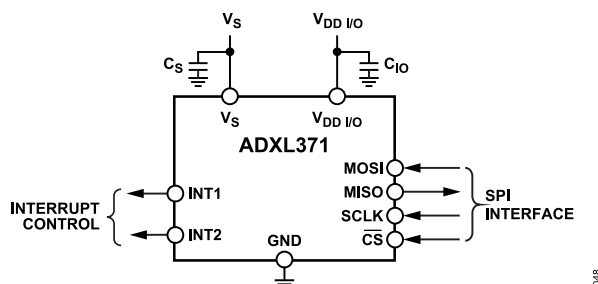Figure 50 shows the recommended bypass capacitors for use with the ADXL371.



*Figure 50. Recommended Bypass Capacitors*

A 0.1 µF ceramic capacitor ($C_S$) at $V_S$ and a 0.1 µF ceramic capacitor ($C_{IO}$) at $V_{DDI/O}$ placed as close as possible to the ADXL371 supply pins are recommended to adequately decouple the accelerometer from noise on the power supply. It is recommended that $V_S$ and $V_{DDI/O}$ be separate supplies to minimize digital clocking noise on the $V_S$ supply. If separating $V_S$ and $V_{DDI/O}$ is not possible, additional filtering of the supplies may be necessary.

If additional decoupling is necessary, a resistor or ferrite bead, no larger than 100 Ω, in series with $V_S$, is recommended. Additionally, increasing the bypass capacitance on $V_S$ to a 1 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor may also improve noise.

Ensure that the connection from the ADXL371 ground to the power supply ground has low impedance because noise transmitted through ground has an effect similar to noise transmitted through $V_S$.

### Power Supply Requirements

The ADXL371 operates using supply voltage rails ranging from 2.5 V to 3.5 V. The operating voltage range ($V_S$) specified in Table 1 ranges from 2.5 V to 3.5 V to account for inaccuracies and transients of up to ±10% on the supply voltage.

When power cycling the ADXL371, it is highly recommended to fully discharge the device to ground level (Vs = 0 V) on each power cycle. If this is not possible, care must be taken regarding the following specifications:

▶ $V_S$ supply start-up threshold
▶ Hold time
▶ Rise time

### $V_{RESET}$

During start-up or power cycling of the ADXL371, any time power is removed from the ADXL371 or falls to less than 1.6 V, the $V_S$ and $V_{DDI/O}$ supplies must be discharged to a reset voltage ($V_{RESET}$) ≤ 100 mV before powering back up. The $V_{RESET}$ specification is a mandatory requirement.

### Hold Time

The $V_S$ and $V_{DDI/O}$ supplies must be held below $V_{RESET}$ for at least 200 ms before powering back up.

### Rise Time

For the worst case scenario ($V_{RESET}$ = 100 mV and hold time = 200 ms), the $V_S$ and $V_{DDI/O}$ supply rise time must be linear and within 250 µs to reach 1.6 V (see Figure 51).



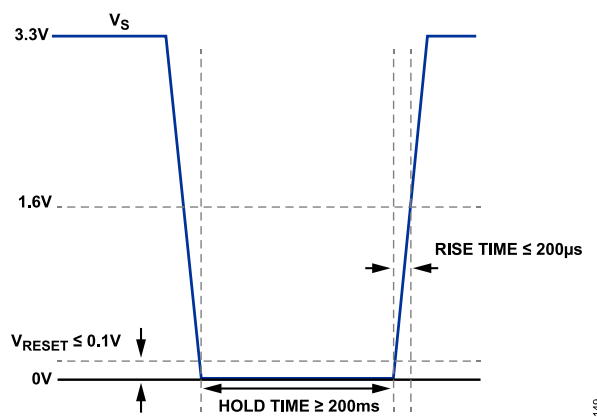*Figure 51. Power Cycling Requirements*

Note that fully discharging the power supply to the ground level allows a longer rise time, ≤600 µs, from 0 V to 1.6 V for a 200 ms hold time.

### Using External Timing Triggers

Figure 52 shows an application diagram for using the INT1 pin as the input for an external clock. In this mode, the external clock determines all accelerometer timing, including the output data rate and bandwidth.

Set the EXT_CLK bit in the TIMING register to enable this feature.
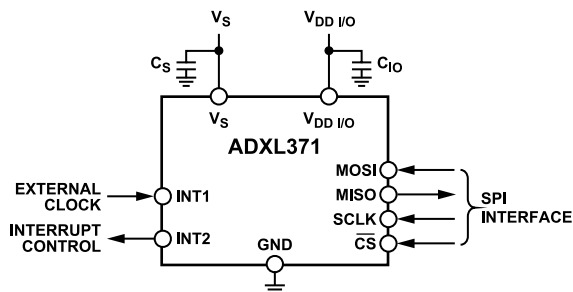
## APPLICATIONS INFORMATION



*Figure 52. INT1 Pin as Input for External Clock*

Figure 53 is an application diagram for using the INT2 pin as a trigger for synchronized sampling. Acceleration samples are produced every time this trigger is activated. Set the EXT_SYNC bit in the TIMING register to enable this feature.
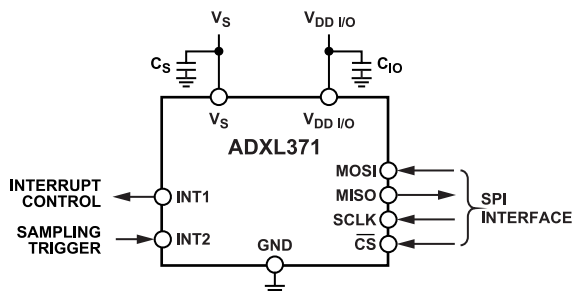


*Figure 53. Using the INT2 Pin to Trigger Synchronized Sampling*

## OPERATION AT VOLTAGES OTHER THAN 3.3 V

The ADXL371 is tested and specified at a supply voltage of $V_S$ = 3.3 V. However, it can be powered with a $V_S$ as high as 3.5 V or as low as 2.5 V. Some performance parameters change as the supply voltage changes, including the supply current, noise, offset, and sensitivity.

## OPERATION AT TEMPERATURES OTHER THAN AMBIENT

The ADXL371 is tested and specified at an ambient temperature. However, it is rated for temperatures between −40°C and +105°C. Some performance parameters change along with temperature, such as offset, sensitivity, clock performance, and current. Some of these temperature variations are characterized in Table 1, and others are shown in the figures within the Typical Performance Characteristics section.

## MECHANICAL CONSIDERATIONS FOR MOUNTING

Mount the ADXL371 on the PCB in a location close to a hard mounting point of the PCB to the case. Mounting the ADXL371 at an unsupported PCB location, as shown in Figure 54, can result in large, apparent measurement errors due to undamped PCB vibration. Locating the accelerometer near a hard mounting point ensures that any PCB vibration at the accelerometer is higher than the mechanical sensor resonant frequency of the accelerometer and, therefore, effectively invisible to the accelerometer. Multiple mounting points, close to the sensor, and/or a thicker PCB also help to reduce the effect of system resonance on the performance of the sensor.
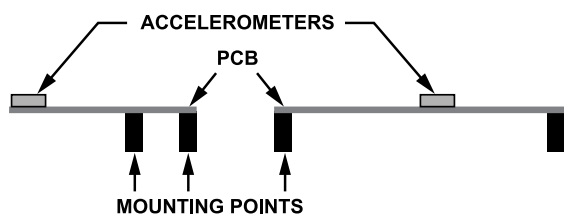


*Figure 54. Incorrectly Placed Accelerometers*
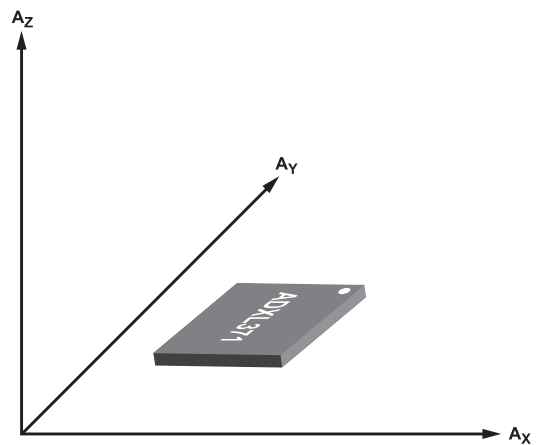
## AXES OF ACCELERATION SENSITIVITY



*Figure 55. Axes of Acceleration Sensitivity (Corresponding Output Increases when Accelerated Along the Sensitive Axis)*
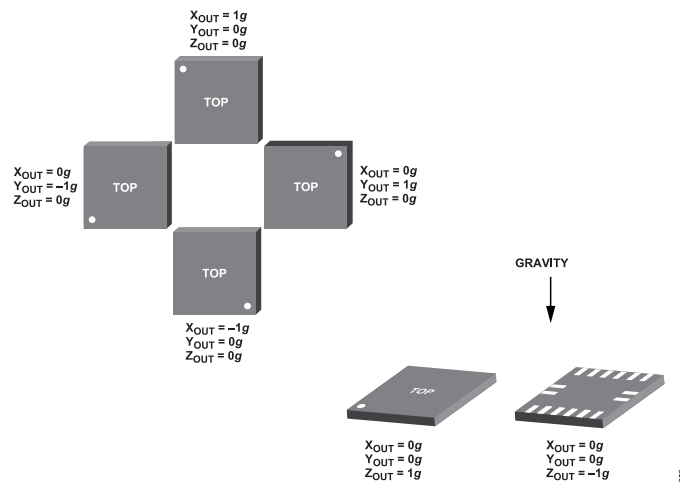
## APPLICATIONS INFORMATION



*Figure 56. Output Response vs. Orientation to Gravity*

## LAYOUT AND DESIGN RECOMMENDATIONS

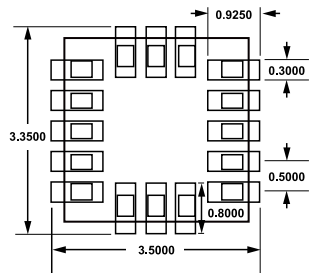Figure 57 shows the recommended printed wiring board land pattern.



*Figure 57. Recommended Printed Wiring Board Land Pattern (Dimensions Shown in Millimeters)*

## SILICON ANOMALY

This anomaly list describes the known bugs, anomalies, and workarounds for the ADXL371.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improving silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

## ADXL371 FUNCTIONALITY ISSUES

*Table 63. ADXL371 Functionality Issues*

| Silicon Revision Identifier | Silicon Status | Anomaly Sheet | Number of Reported Anomalies |
|---|---|---|---|
| REVID = 0xFB | Released | Rev. 0 | 1 |

## FUNCTIONALITY ISSUE

*Table 64. FIFO Error [er001]*

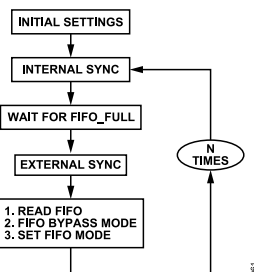| | |
|---|---|
| **Background** | Data must be stored in the FIFO as an x, y, z, x, y, z, … sequence. |
| **Issue** | In all FIFO modes, data misalignment occurs. Data may be stored in the FIFO as a y, z, x, y, z, x, … sequence or a z, x, y, z, x, y, … sequence. |
| **Workaround** | Leverage the external trigger synchronization function to disable the sensor ADC before accessing the FIFO (see Figure 58 for an implementation example). <br> To initialize, follow these steps: <br> 1. Set the desired FIFO mode and other desired configurations. <br> 2. Set the timing register (0x3D) to external sync along with the ODR. Do not apply an external trigger signal to INT2 to keep the ADC off. <br> 3. Set the device to measurement mode. <br> For the main loop, follow these steps: <br> 1. Set the timing register (0x3D) to internal sync along with the ODR. <br> 2. Wait for the FIFO_FULL interrupt from INT1. <br> 3. Set the timing register (0x3D) to external sync along with the ODR. <br> 4. Read the entire contents of the FIFO. <br> 5. Clear the FIFO (bypass mode). <br> 6. Set the desired FIFO mode. |
| **Related Issues** | None. |



*Figure 58. FIFO Workaround Implementation Example*
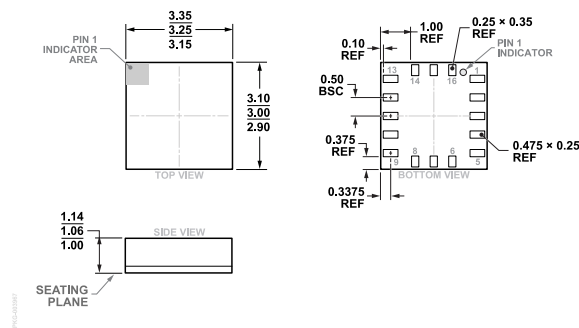
## OUTLINE DIMENSIONS



*Figure 59. 16-Terminal Land Grid Array [LGA]*
*(CC-16-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Quantity |
|---|---|---|---|---|
| ADXL371BCCZ-RL | −40°C to +105°C | 16-Terminal Land Grid Array [LGA] | CC-16-4 | 5000 |
| ADXL371BCCZ-RL7 | −40°C to +105°C | 16-Terminal Land Grid Array [LGA] | CC-16-4 | 1500 |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model[1] | Description |
|---|---|
| EVAL-ADXL371Z | Evaluation Board |

[1] Z = RoHS Compliant Part.

$I^2C$ refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).