ICG-20660

High Performance 6-Axis OIS/EIS Optimized MEMS Sensor

GENERAL DESCRIPTION

The ICG-20660 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, in a small 3 mm x 3 mm x 0.75 mm (16-pin LGA) package.

- High performance specs
  - Gyroscope sensitivity error: ±3%
  - Gyroscope noise: 6.5mdps/√Hz
- Includes 512-byte FIFO to reduce traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode
- EIS FSYNC support

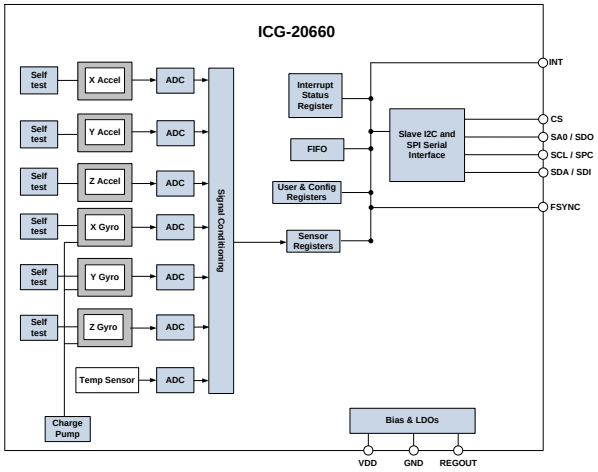
The ICG-20660 includes on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features an operating voltage range down to 1.71 V. Communication ports include I^2C and high speed SPI at 7 MHz.

ORDERING INFORMATION

PART	AXES	TEMP RANGE	PACKAGE
ICG-20660†	X,Y,Z	-40°C to +85°C	16-Pin LGA

†Denotes RoHS and Green-Compliant Package

BLOCK DIAGRAM



APPLICATIONS

- OIS (Optical Image Stabilization) in phone camera modules, DSLR, and DSC
- EIS (Electronic Image Stabilization) in DSC, and phone camera modules

FEATURES

- ±3% Gyro initial sensitivity
- 3-Axis optimized OIS/EIS programmable gyro FSR of ±125 dps, ±250 dps, ±500 dps, and ±250 dps
- 3-Axis Accelerometer with Programmable FSR of ±2*g*, ±4*g*, ±8*g*, and ±16*g*
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- 512-byte FIFO buffer enables the applications processor to read the data in bursts
- On-Chip 16-bit ADCs and Programmable Filters
- Host interface: 7 MHz SPI or 400 kHz Fast Mode I^2C
- Digital-output temperature sensor
- VDD operating range of 1.71 V to 3.45 V
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

TYPICAL OPERATING CIRCUIT

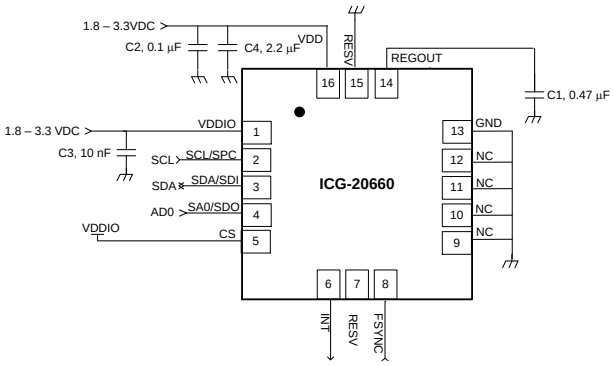


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document provides a description, specifications, and design-related information on the ICG-20660 MotionTracking device for imaging applications, such as Optical Image Stabilization, OIS, or Electronic Image Stabilization, EIS. The device is housed in a small 3 mm x 3 mm x 0.75 mm 16-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICG-20660 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 3 mm x 3 mm x 0.75 mm (16-pin LGA) package. The 6-axis sensor allows efficient implementation of advanced 5- and 6-axes Optical Image Stabilization in high-end still and video cameras. It also features a 512-byte FIFO for EIS applications to lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data for a given video frame. The unique support for FSYNC (frame sync), facilitates synchronization of Video Frame Sync from Image sensors and Motion data from the gyroscopes and accelerators collected during a given frame via an interrupt to the host. ICG-20660, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices.

The gyroscope has a programmable full-scale range of ±125 dps, ±250 dps, and ±500 dps, optimized for Image Stabilization applications. The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 V to 3.6 V, and a separate digital IO supply, VDDIO from 1.71 V to 3.6 V.

Communication with all registers of the device is performed using either I^2C at 400 kHz or SPI at 7 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x0.75 mm (16-pin LGA), to provide a very small yet high-performance, low-cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.3 APPLICATIONS

- *OIS,* Optical Image Stabilization in phone camera modules, DSLR, and DSC
- *EIS,* Electronic Image Stabilization in DSC, and phone camera modules

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICG-20660 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±125 dps, ±250 dps, and ±500 dps and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICG-20660 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g* and integrated 16-bit ADCs
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

The ICG-20660 includes the following additional features:

- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- 512-byte FIFO buffer enable the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temp sensor
- 10,000*g* shock tolerant
- 400 kHz Fast Mode I^2C for communicating with all registers
- 7 MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL = 0		±125		dps	3
	FS_SEL = 1		±250		dps	3
	FS_SEL = 2		±500		dps	3
ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL = 0		262		LSB/(dps)	3
	FS_SEL = 1		131		LSB/(dps)	3
	FS_SEL = 2		65.5		LSB/(dps)	3
Initial Sensitivity Scale Factor Tolerance	25°C		±3		%	2
Sensitivity Scale Factor Variation Over Temperature	-20°C to +75°C		±3		%	1
Nonlinearity	Best fit straight line; 25°C		±0.1		%	1
Cross-Axis Sensitivity			±5		%	1
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±5		dps	2
ZRO Variation Over Temperature	-20°C to +75°C		±5		dps	1
GYROSCOPE NOISE PERFORMANCE (FS_SEL = 0)						
Total RMS Noise	DLPFCFG = 2 (92 Hz)		0.075		dps-rms	2
	DLPFCFG = 1 (176 Hz)		0.10		dps-rms	2
	DLPFCFG = 0 (250 Hz)		0.12		dps-rms	2
Total Peak-to-Peak Noise	DLPFCFG = 2 (92 Hz)		0.37		dps-p-p	2
	DLPFCFG = 1 (176 Hz)		0.50		dps-p-p	2
	DLPFCFG = 0 (250 Hz)		0.60		dps-p-p	2
Rate Noise Spectral Density	At 10 Hz		0.0065		dps /√Hz	4
GYROSCOPE MECHANICAL Mechanical Frequency Sensor Mechanical Bandwidth		 25.6 1.2	 27	 29	 kHz kHz	 2 1
LOW PASS FILTER RESPONSE	Programmable Range	92		250	Hz	3
GYROSCOPE START-UP TIME			80		ms	1
OUTPUT DATA RATE	Programmable, Normal (Filtered) mode	1000		8000	Hz	1

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.
4. Calculated from Total RMS Noise.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	AFS_SEL = 0		±2		*g*	3
	AFS_SEL = 1		±4		*g*	3
	AFS_SEL = 2		±8		*g*	3
	AFS_SEL = 3		±16		*g*	3
ADC Word Length	Output in two's complement format		16		bits	3
Sensitivity Scale Factor	AFS_SEL = 0		16,384		LSB/*g*	3
	AFS_SEL = 1		8,192		LSB/*g*	3
	AFS_SEL = 2		4,096		LSB/*g*	3
	AFS_SEL = 3		2,048		LSB/*g*	3
Sensitivity Initial Tolerance	Component-level		±1		%	2
Sensitivity Change vs. Temperature	-20°C to +75°C AFS_SEL = 0 Component-level		±2.5		%	1
Nonlinearity	Best Fit Straight Line		±0.5		%	1
Cross-Axis Sensitivity			±2		%	1
ZERO-G OUTPUT						
Initial Tolerance	Component-level, X and Y axes		±40		m*g*	2
	Component-level, Z axis		±65		mg	2
Zero-G Level Change vs. Temperature	-20°C to +75°C		±50		m*g*	1
NOISE PERFORMANCE						
Power Spectral Density			220		µ*g*/√Hz	4
Total RMS Noise	DLPFCFG = 2 (100 Hz)		2		mg-rms	2
LOW PASS FILTER RESPONSE	Programmable Range	5		260	Hz	3
INTELLIGENCE FUNCTION INCREMENT			4		m*g*/LSB	3
ACCELEROMETER STARTUP TIME	From Sleep mode		20		ms	1
	From Cold Start, 1ms VDD ramp		30		ms	1
OUTPUT DATA RATE	Low power (duty-cycled)	0.24		500	Hz	1
	Duty-cycled, over temp		±15		%	
	Low noise (active)	4		4000	Hz	

Table 2. Accelerometer Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.
4. Calculated from Total RMS Noise.

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	1
VDDIO		1.71	1.8	3.45	V	1
SUPPLY CURRENTS & BOOT TIME						
Active Current	6-Axis Gyroscope + Accelerometer		3		mA	1
Accelerometer Low -Power Mode (Gyroscope disabled)	100 Hz ODR, 1x averaging		57		µA	2
Full-Chip Sleep Mode			10		µA	1
Boot Time	VDD on to first register write		50		ms	1
TEMPERATURE RANGE						
Operating Temperature Range		-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Based on simulation.

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.1		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Room Temperature Offset	25°C		0		°C	1
Sensitivity	Untrimmed		326.8		LSB/°C	1
Power-On RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01	20	100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
I²C ADDRESS	SA0 = 0 SA0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SA0, SPC, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD} = 1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD} = 1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN = 1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN = 1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN = 0		50		µs	
I2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B = 1,2,3 SMPLRT_DIV = 0		32		kHz	2
	FCHOICE_B = 0; DLPFCFG = 0 or 7 SMPLRT_DIV = 0		8		kHz	2
	FCHOICE_B = 0; DLPFCFG = 1,2,3,4,5,6; SMPLRT_DIV = 0		1		kHz	2
Clock Frequency Initial Tolerance	CLK_SEL= 0, 6 or gyro inactive; 25°C	-5		+5	%	1

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
	CLK_SEL = 1,2,3,4,5 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL = 0,6 or gyro inactive	-10		+10	%	1
	CLK_SEL = 1,2,3,4,5 and gyro active		±1		%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.

3.3.3 Other Electrical Specifications

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	1
	High Speed Characterization		1	7	MHz	1, 2
SPI Modes			Modes 0 and 3			
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 5. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 7 MHz operation.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Table 6. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.

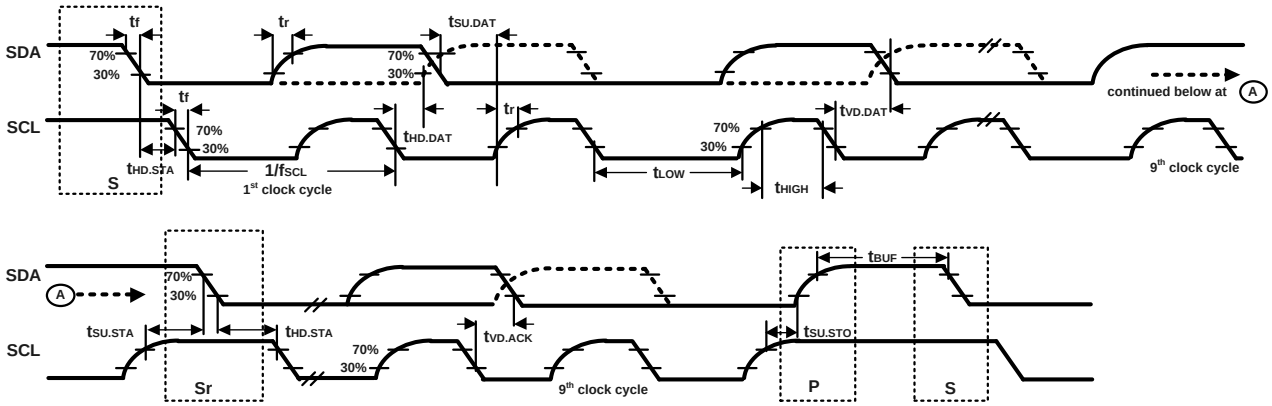


Figure 1. I²C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				7	MHz	
t_{LOW}, SCLK Low Period		64			ns	
t_{HIGH}, SCLK High Period		64			ns	
$t_{SU.CS}$, CS Setup Time		8			ns	
$t_{HD.CS}$, CS Hold Time		500			ns	
$t_{SU.SDI}$, SDI Setup Time		5			ns	
$t_{HD.SDI}$, SDI Hold Time		7			ns	
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			59	ns	
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	6			ns	
$t_{DIS.SDO}$, SDO Output Disable Time				50	ns	

Table 7. SPI Timing Characteristics (7 MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.

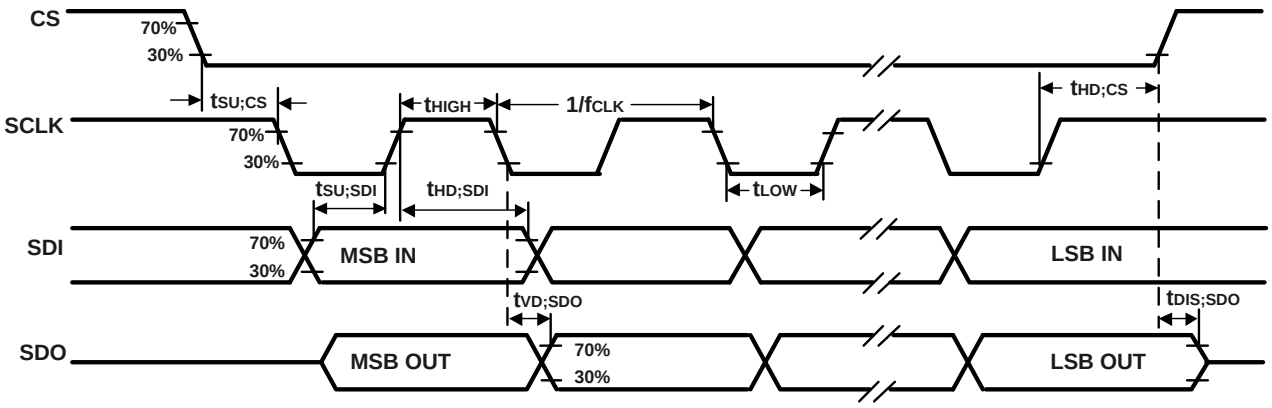


Figure 2. SPI Bus Timing Diagram

3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
REGOUT	-0.5 V to 2 V
Input Voltage Level (SA0, FSYNC, SCL, SDA)	-0.5 V to VDD + 0.5 V
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2 ms
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 250 V (MM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 8. Absolute Maximum Ratings

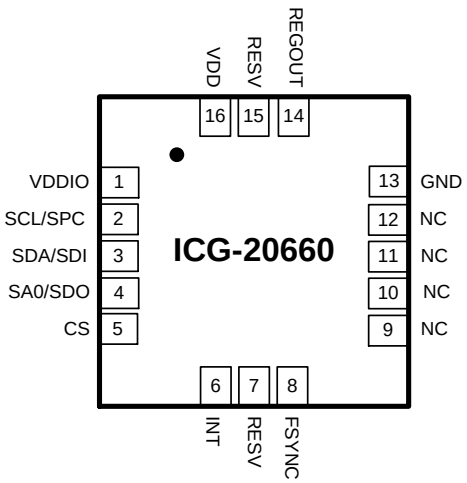
4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

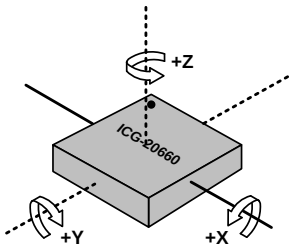
Pin Number	Pin Name	Pin Description
1	VDDIO	Digital I/O supply voltage
2	SCL/SPC	I²C serial clock (SCL); SPI serial clock (SPC)
3	SDA/SDI	I²C serial data (SDA); SPI serial data input (SDI)
4	SA0/SDO	I²C slave address LSB (SA0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode; 1 = I²C mode)
6	INT	Interrupt digital output (totem pole or open-drain)
7	RESV	Reserved. Do not connect.
8	FSYNC	Synchronization digital input (optional). Connect to GND if unused.
9	NC	Connect to GND or do not connect
10	NC	Connect to GND or do not connect
11	NC	Connect to GND or do not connect
12	NC	Connect to GND or do not connect
13	GND	Connect to GND
14	REGOUT	Regulator filter capacitor connection
15	RESV	Reserved. Connect to GND
16	VDD	Power Supply

Table 9. Signal Descriptions

Note: VDD, VDDIO, SCL/SPC and CS pins must be correctly managed at power-up to guarantee proper device start-up. Please refer to sections 4.18 and 4.19 for detailed power-up instructions.



LGA Package (Top View)
16-pin, 3mm x 3mm x 0.75 mm
Typical Footprint and thickness



Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin out Diagram for ICG-20660 3 mm x 3 mm x0.75 mm LGA

4.2 TYPICAL OPERATING CIRCUIT

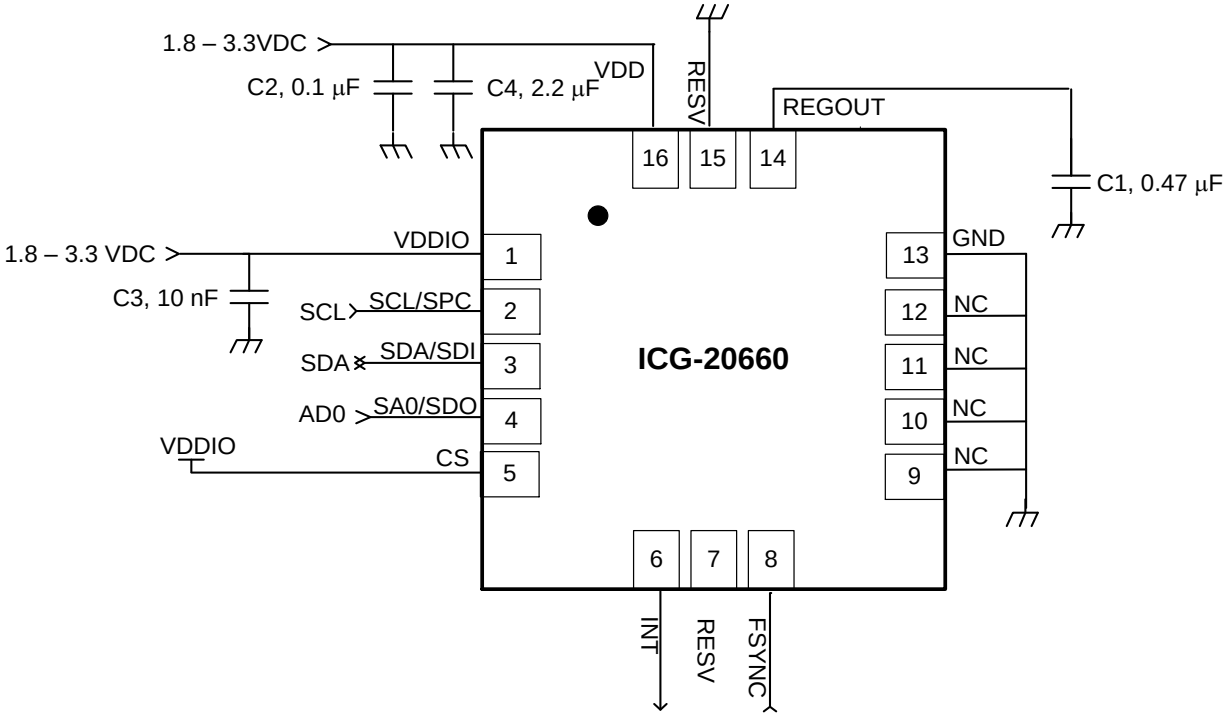


Figure 4. ICG-20660 LGA Application Schematic

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
REGOUT Capacitor	C1	Ceramic, X7R, 0.47 µF ±10%, 2 V	1
VDD Bypass Capacitors	C2	Ceramic, X7R, 0.1 µF ±10%, 4 V	1
	C4	Ceramic, X7R, 2.2 µF ±10%, 4 V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10 nF ±10%, 4 V	1

Table 10. Bill of Materials

4.4 BLOCK DIAGRAM

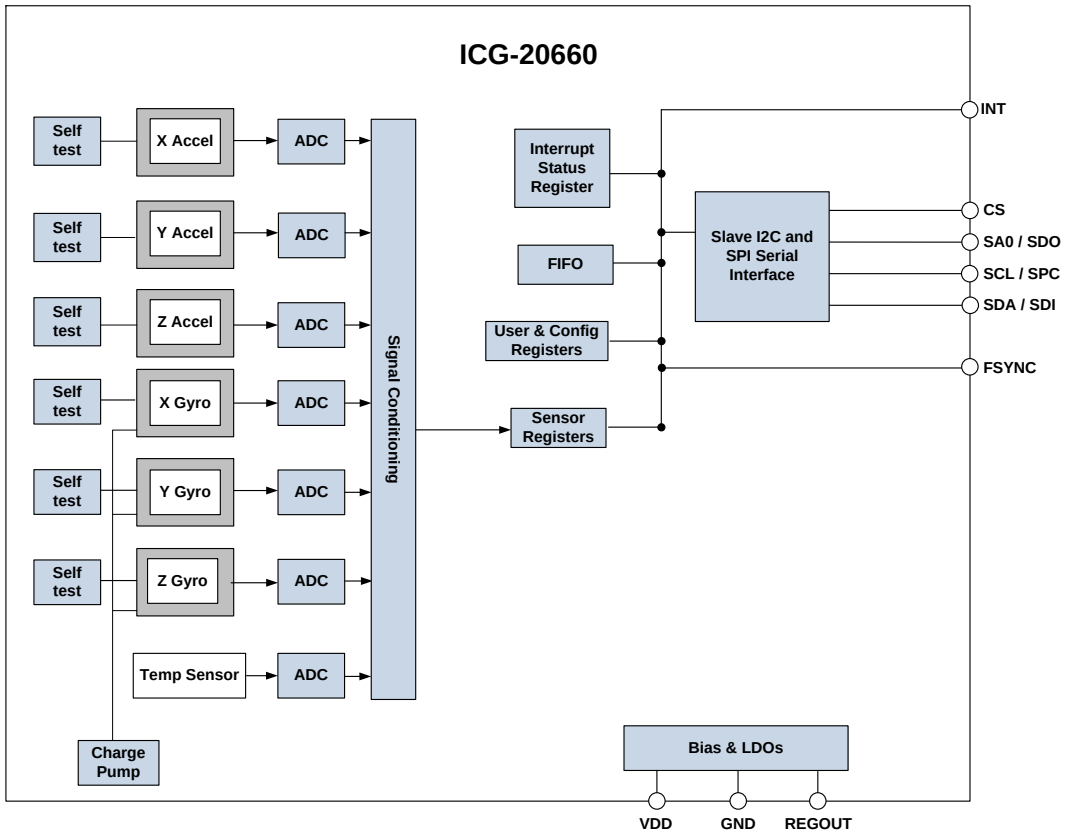


Figure 5. ICG-20660 Block Diagram

4.5 OVERVIEW

The ICG-20660 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICG-20660 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±125, ±250, or ±500 degrees per second (dps). The ADC sample rate is programmable up to 8,000 samples per second with user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICG-20660's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICG-20660's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g*.

4.8 I²C AND SPI SERIAL COMMUNICATIONS INTERFACES

The ICG-20660 communicates to a system processor using either a SPI or an I²C serial interface. The ICG-20660 always acts as a slave when communicating to the system processor. The LSB of the I²C slave address is set by pin 4 (SA0).

4.8.1 ICG-20660 Solution Using I²C Interface

In the figure below, the system processor is an I²C master to the ICG-20660.

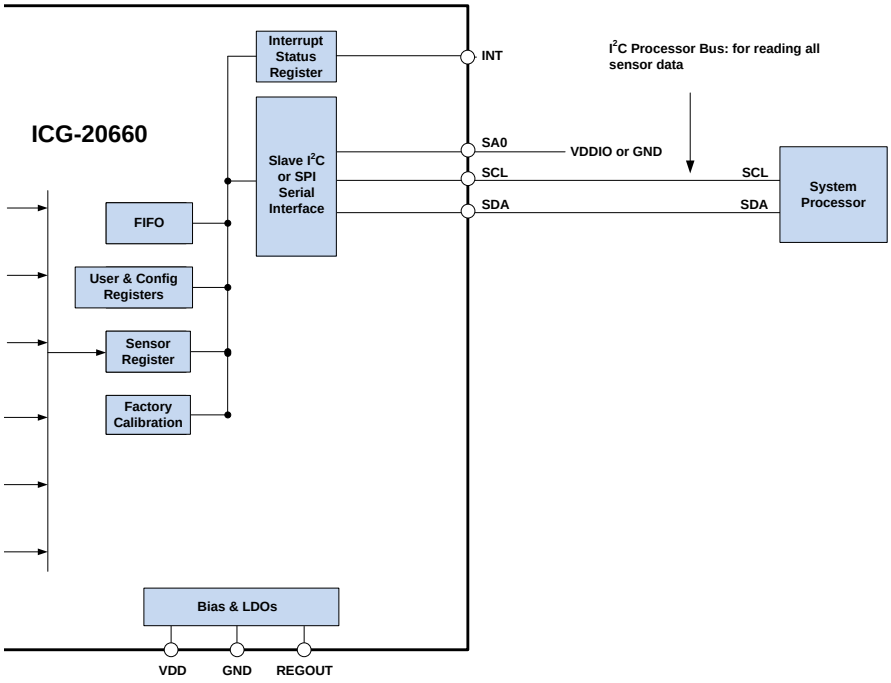


Figure 6. ICG-20660 Solution Using I²C Interface

4.8.2 ICG-20660 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ICG-20660. Pins 2, 3, 4, and 5 are used to support the SPC, SDI, SDO, and CS signals for SPI communications.

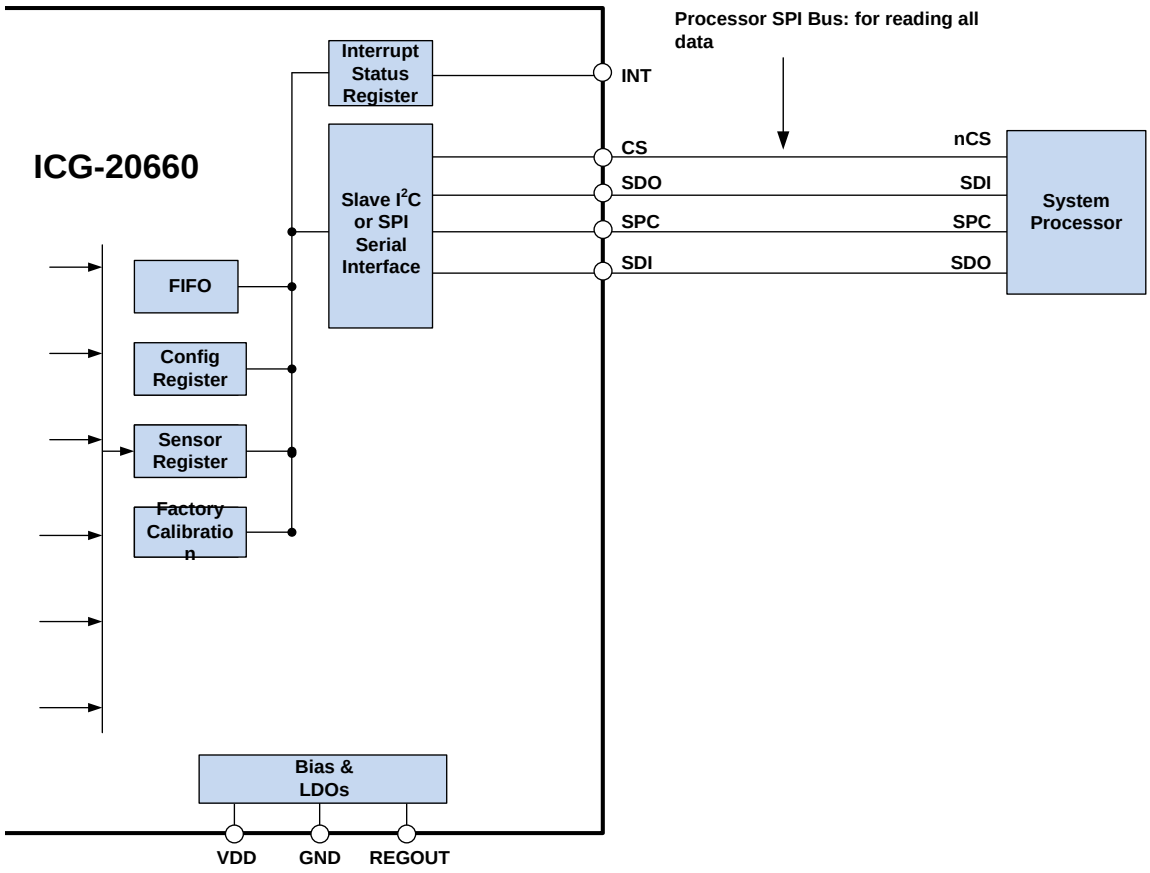


Figure 7. ICG-20660 Solution Using SPI Interface

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers (registers 27 and 28).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

SELF-TEST RESPONSE = SENSOR OUTPUT WITH SELF-TEST ENABLED – SENSOR OUTPUT WITH SELF-TEST DISABLED

The self-test response for each gyroscope axis is defined in the gyroscope specification table, while that for each accelerometer axis is defined in the accelerometer specification table.

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test. It is recommended to use InvenSense MotionApps software for executing self-test.

For further information on Self-Test please refer to the register map of ICG-20660.

4.10 CLOCKING

The ICG-20660 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator

b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 FIFO

The ICG-20660 contains a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

The ICG-20660 allows FIFO read in low-power accelerometer mode.

For further information regarding the FIFO, please refer to the register map of ICG-20660.

4.13 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.14 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICG-20660 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.15 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICG-20660. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.16 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.17 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICG-20660.

Mode	Name	Gyro	Accel
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Low-Power Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
7	6-Axis Low-Noise Mode	On	On

Table 11. Standard Power Modes for ICG-20660

Notes:

1. Power consumption for individual modes can be found in section 0.

4.18 POWER-UP SEQUENCE

When applying VDD, the power voltage ramp is detected and a power-on-reset sequence is triggered inside the component. During this phase the device starts operating and internal logic levels are defined. For proper component initialization the power-up should be performed with both CS and SCL/SPC low, ensuring that CS and SCL pins are not in an undetermined state during the VDD ramp. If starting in I^2C mode (CS at logic high), power-up should be performed with SCL/SPC low. Power-up with SCL/SPC high is not a supported case and must be avoided.

It is worth noting that if the I/O pins (e.g. CS, SCL/SPC) are between V_{IL} and V_{IH} when the power-on-reset sequence is triggered, their value is undetermined and the internal logic levels may not be properly defined. It should also be noted that V_{IL} and V_{IH} are related to VDDIO and their value changes at power-up according to the applied VDDIO voltage ramp.

Power-up sequences that do not respect the conditions above may not lead to proper digital interface initialization. In this case a preliminary soft reset operation (PWR_MGMT_1 register set 0x81) must be performed to reset the digital interface, as soon as both VDD and VDDIO are stable at their final voltage. Since the digital interface may not be properly initialized, the device may not provide the acknowledge signal if the I^2C protocol is used.

4.19 SENSOR INITIALIZATION AND CLOCK SOURCE SELECTION

When power-up sequence is completed (as per section 4.18), a soft reset is required to initialize the sensor and let the device select the best clock source. The soft reset must be performed by setting the register PWR_MGMT_1 (address 0x6B) to 0x81, prior to registers initialization.

Soft reset must be performed as first operation after the power-up sequence to ensure the proper component registers setting.

Correct WHOAMI value is ensured only after the soft reset has been completed.

5 PROGRAMMABLE INTERRUPTS

The ICG-20660 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

Interrupt Name	Module
Motion Detection	Motion
FIFO Overflow	FIFO
Data Ready	Sensor Registers

Table 12. Table of Interrupt Sources

For information regarding the interrupt enable/disable registers and flag registers, please refer to the register map of ICG-20660 in this document.

6 DIGITAL INTERFACE

6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICG-20660 can be accessed using either I²C at 400 kHz or SPI at 7 MHz. SPI operates in four-wire mode.

Pin Number	Pin Name	Pin Description
1	VDDIO	Digital I/O supply voltage.
4	SA0 / SDO	I²C Slave Address LSB (SA0); SPI serial data output (SDO)
2	SCL / SPC	I²C serial clock (SCL); SPI serial clock (SPC)
3	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)

Table 13. Serial Interface

Note: To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 6.3.

For further information regarding the *I2C_IF_DIS* bit, please refer to the register map of ICG-20660.

6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICG-20660 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICG-20660 is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin SA0. This allows two ICG-20660s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin SA0 is logic low) and the address of the other should be b1101001 (pin SA0 is logic high).

6.3 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

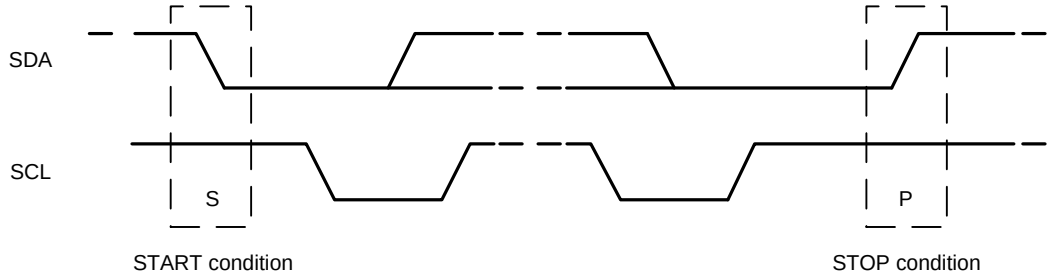


Figure 8. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

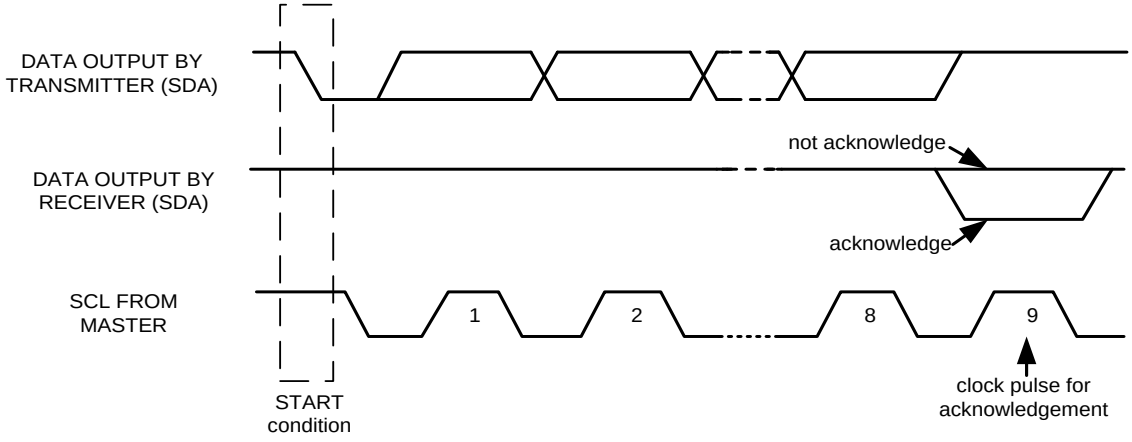


Figure 9. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

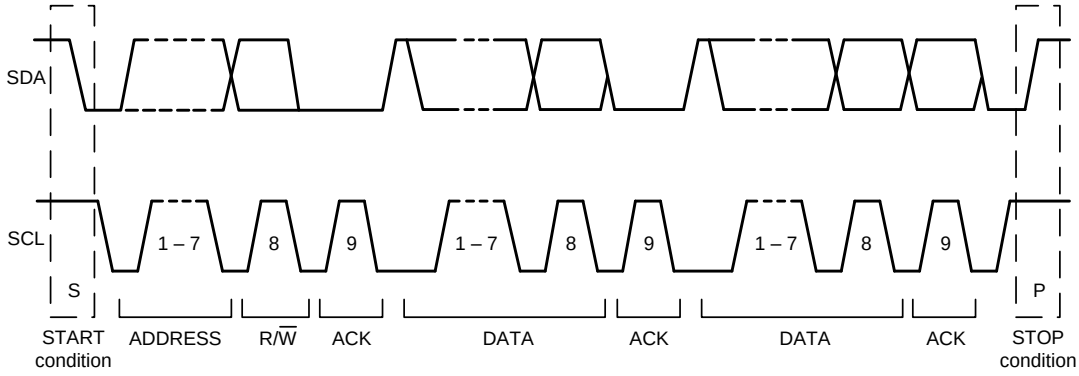


Figure 10. Complete I²C Data Transfer

To write the internal ICG-20660 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICG-20660 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICG-20660 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICG-20660 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICG-20660 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICG-20660, the master transmits a start signal followed by the slave address and read bit. As a result, the ICG-20660 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I²C TERMS

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICG-20660 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 14. I²C Terms

6.5 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ICG-20660 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SPC), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last.
2. Data is latched on the rising edge of SPC.
3. Data should be transitioned on the falling edge of SPC.
4. The maximum frequency of SPC is 7 MHz.
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

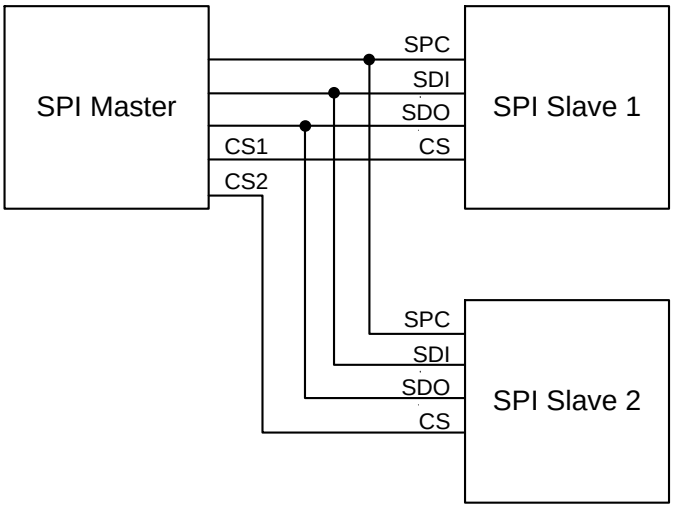


Figure 11. Typical SPI Master/Slave Configuration

7 SERIAL INTERFACE CONSIDERATIONS

7.1 ICG-20660 SUPPORTED INTERFACES

The ICG-20660 supports I^2C communications on its serial interface.

The ICG-20660's I/O logic levels are set to be VDDIO.

The figure below depicts a sample circuit of ICG-20660. It shows the relevant logic levels and voltage connections.

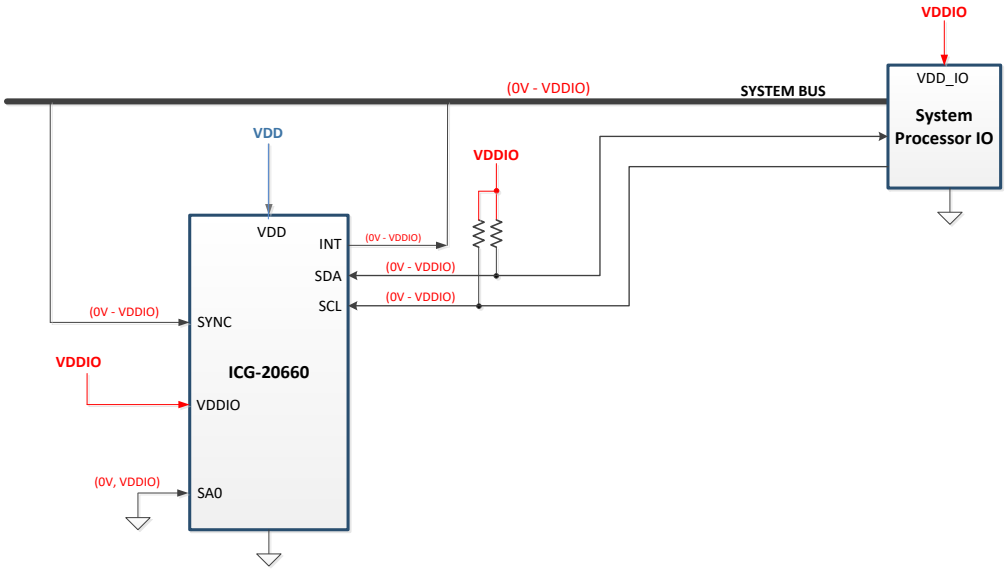


Figure 12. I/O Levels and Connections

8 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

8.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

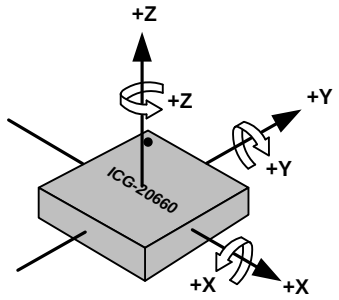


Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation

8.2 PACKAGE DIMENSIONS

16 Lead LGA (3 mm x 3 mm x 0.75 mm) NiAu pad finish

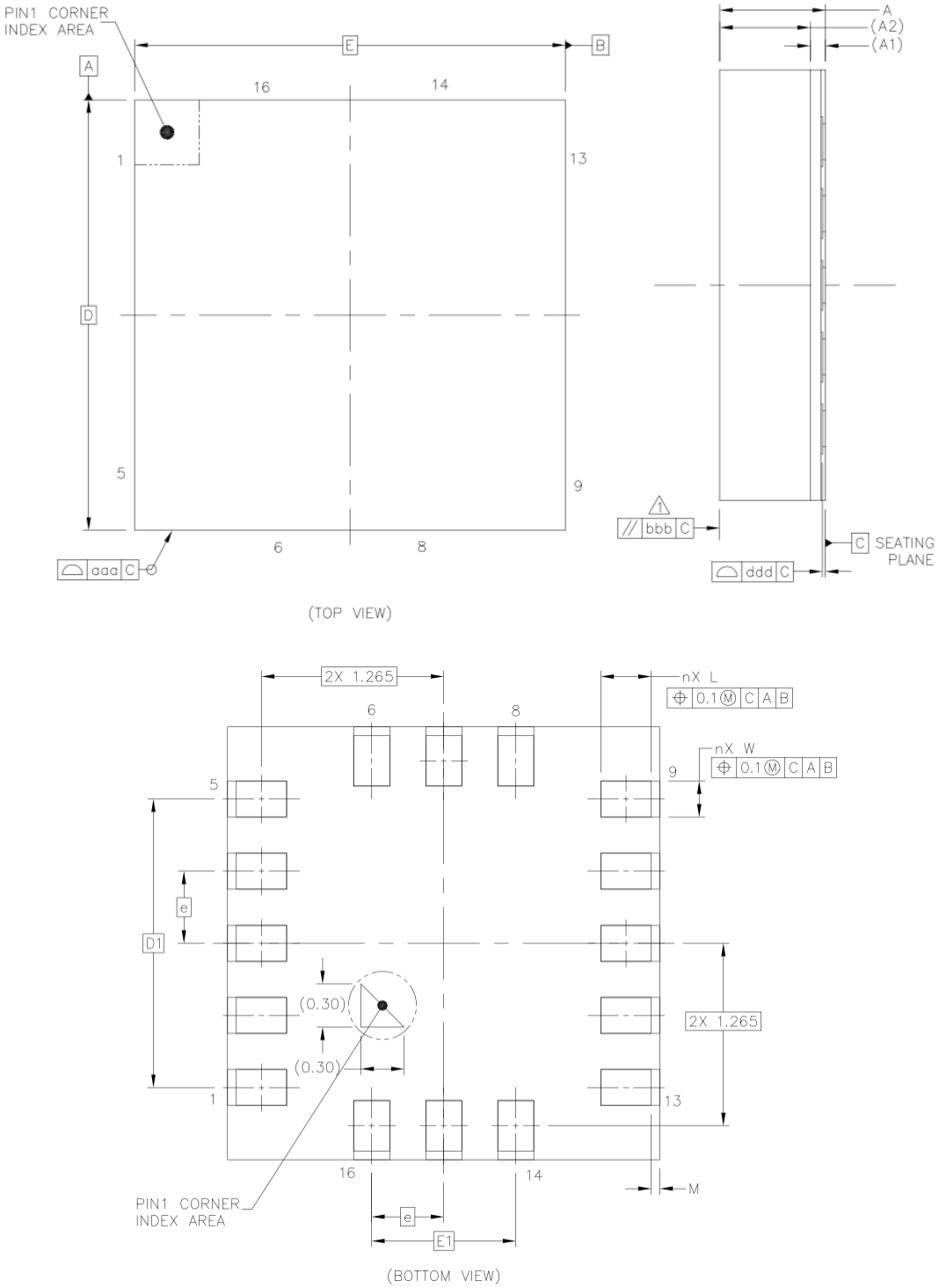


Figure 14. Package Dimensions

	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.7	0.75	0.8
Substrate Thickness	A1		0.105 REF	
Mold Thickness	A2		0.63 REF	
Body Size	D	2.9	3	3.1
	E	2.9	3	3.1
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.3	0.35	0.4
Lead Pitch	e		0.5 BSC	
Lead Count	n		16	
Edge Ball Center to Center	D1		2 BSC	
	E1		1 BSC	
Body Center to Contact Ball	SD		---	
	SE		---	
Ball Width	b	---	---	---
Ball Diameter			---	
Ball Opening			---	
Ball Pitch	e1		---	
Ball Count	n1		---	
Pre-Solder		---	---	---
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		---	
Ball Offset (Ball)	fff		---	
Lead Edge to Package Edge	M	0.01	0.06	0.11

9 PART NUMBER PACKAGE MARKING

The part number package marking for ICG-20660 devices is summarized below:

Part Number	Part Number Package Marking
ICG-20660	IC2660

10 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

11 REGISTER MAP

The following table lists the register map for the ICG-20660.

The device will come up in sleep mode upon power-up. In order to take the device out of the sleep mode set the PWR_MGMT_1[6] = 0 in register 107 (sleep mode bit in power management register).

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Accessible in Sleep and LPA Modes?	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	00	SELF_TEST_X_GYRO	READ/ WRITE	N	XG_ST_DATA[7:0]							
01	01	SELF_TEST_Y_GYRO	READ/ WRITE	N	YG_ST_DATA[7:0]							
02	02	SELF_TEST_Z_GYRO	READ/ WRITE	N	ZG_ST_DATA[7:0]							
04	04	XG_OFFS_TC_H	READ/ WRITE	N	-	-	-	-	-	-	XG_OFFS_TC _H [9]	XG_OFFS_TC _H [8]
05	05	XG_OFFS_TC_L	READ/ WRITE	N	XG_OFFS_TC_L [7:0]							
07	07	YG_OFFS_TC_H	READ/ WRITE	N	-	-	-	-	-	-	YG_OFFS_TC _H [9]	YG_OFFS_TC _H [8]
08	08	YG_OFFS_TC_L	READ/ WRITE	N	YG_OFFS_TC_L [7:0]							
0A	10	ZG_OFFS_TC_H	READ/ WRITE	N	-	-	-	-	-	-	ZG_OFFS_TC _H [9]	ZG_OFFS_TC _H [8]
0B	11	ZG_OFFS_TC_L	READ/ WRITE	N	ZG_OFFS_TC_L [7:0]							
0D	13	SELF_TEST_X_ACCEL	READ/ WRITE	N	XA_ST_DATA[7:0]							
0E	14	SELF_TEST_Y_ACCEL	READ/ WRITE	N	YA_ST_DATA[7:0]							
0F	15	SELF_TEST_Z_ACCEL	READ/ WRITE	N	ZA_ST_DATA[7:0]							
13	19	XG_OFFS_USRH	READ/ WRITE	N	X_OFFS_USR [15:8]							
14	20	XG_OFFS_USRL	READ/ WRITE	N	X_OFFS_USR [7:0]							
15	21	YG_OFFS_USRH	READ/ WRITE	N	Y_OFFS_USR [15:8]							
16	22	YG_OFFS_USRL	READ/ WRITE	N	Y_OFFS_USR [7:0]							
17	23	ZG_OFFS_USRH	READ/ WRITE	N	Z_OFFS_USR [15:8]							
18	24	ZG_OFFS_USRL	READ/ WRITE	N	Z_OFFS_USR [7:0]							
19	25	SMPLRT_DIV	READ/ WRITE	Y	SMPLRT_DIV[7:0]							
1A	26	CONFIG	READ/ WRITE	N	-	FIFO_ MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	READ/ WRITE	N	XG_ST	YG_ST	ZG_ST	FS_SEL [1:0]		-	FCHOICE_B[1:0]	
1C	28	ACCEL_CONFIG	READ/ WRITE	N	XA_ST	YA_ST	ZA_ST	ACCEL_FS_SEL[1:0]		-		
1D	29	ACCEL_CONFIG 2	READ/ WRITE	Y	FIFO_SIZE		DEC2_CFG		ACCEL_FCHOI CE_B	A_DLPF_CFG		
1E	30	LP_MODE_CFG	R/W	N	-	-	-	-	-	LPOSC_CLKSEL		
1F	31	ACCEL_WOM_THR	R/W	N	WOM_THR[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Accessible in Sleep and LPA Modes?	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23	35	FIFO_EN	READ/ WRITE	N	TEMP _FIFO_EN	XG_FIFO_EN	YG_FIFO_EN	ZG_FIFO_EN	ACCEL_FIFO_ EN	-	-	-
36	54	FSYNC_INT	READ to CLEAR	N	FSYNC_INT	-	-	-	-	-	-	-
37	55	INT_PIN_CFG	READ/ WRITE	Y	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_INT_L EVEL	FSYNC _INT_MODE_ EN	-	-
38	56	INT_ENABLE	READ/ WRITE	Y	WOM_EN			FIFO _OFLOW _EN	-	-	-	DATA_RDY_I NT_EN
3A	58	INT_STATUS	READ to CLEAR	N	WOM_X_IN T	WOM_Y_INT	WOM_Z_INT	FIFO _OFLOW _INT	-	-	-	DATA _RDY_INT
3B	59	ACCEL_XOUT_H	READ	N	ACCEL_XOUT_H[15:8]							
3C	60	ACCEL_XOUT_L	READ	N	ACCEL_XOUT_L[7:0]							
3D	61	ACCEL_YOUT_H	READ	N	ACCEL_YOUT_H[15:8]							
3E	62	ACCEL_YOUT_L	READ	N	ACCEL_YOUT_L[7:0]							
3F	63	ACCEL_ZOUT_H	READ	N	ACCEL_ZOUT_H[15:8]							
40	64	ACCEL_ZOUT_L	READ	N	ACCEL_ZOUT_L[7:0]							
41	65	TEMP_OUT_H	READ	N	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	READ	N	TEMP_OUT[7:0]							
43	67	GYRO_XOUT_H	READ	N	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	READ	N	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	READ	N	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	READ	N	GYRO_YOUT[7:0]							
47	71	GYRO_ZOUT_H	READ	N	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT_L	READ	N	GYRO_ZOUT[7:0]							
68	104	SIGNAL_PATH_RESET	READ/ WRITE	N	-	-	-	-	-	-	ACCEL _RST	TEMP _RST
69	105	ACCEL_INTEL_CTRL	READ/ WRITE	N	ACCEL_INTE L_EN	ACCEL_INTEL _MODE	-		-		--	--
6A	106	USER_CTRL	READ/ WRITE	N	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RST	-	SIG_COND _RST
6B	107	PWR_MGMT_1	READ/ WRITE	Y	DEVICE_RES ET	SLEEP	CYCLE	GYRO_ STANDBY	TEMP_DIS	CLKSEL[2:0]		
6C	108	PWR_MGMT_2	READ/ WRITE	Y	FIFO_LP_EN	-	STBY_XA	STBY_YA	STBY_ZA	STBY_XG	STBY_YG	STBY_ZG
72	114	FIFO_COUNTH	READ	Y	-			FIFO_COUNT[12:8]				
73	115	FIFO_COUNTL	READ	Y	FIFO_COUNT[7:0]							
74	116	FIFO_R_W	READ/ WRITE	Y	FIFO_DATA[7:0]							
75	117	WHO_AM_I	READ	N	WHOAMI[7:0]							
77	119	XA_OFFSET_H	READ/ WRITE	N	XA_OFFS [14:7]							
78	120	XA_OFFSET_L	READ/ WRITE	N	XA_OFFS [6:0]							-
7A	122	YA_OFFSET_H	READ/ WRITE	N	YA_OFFS [14:7]							
7B	123	YA_OFFSET_L	READ/ WRITE	N	YA_OFFS [6:0]							-
7D	125	ZA_OFFSET_H	READ/ WRITE	N	ZA_OFFS [14:7]							
7E	126	ZA_OFFSET_L	READ/ WRITE	N	ZA_OFFS [6:0]							-

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the ACCEL_XOUT_H register (Register 59) contains the 8 most significant bits, *ACCEL_XOUT*[15:8], of the 16-bit X-Axis accelerometer measurement, *ACCEL_XOUT*.

The reset value is 0x00 for all registers other than the registers below, also the self-test registers contain pre-programmed values and will not be 0x00 after reset.

- Register 107 (0x01) Power Management 1
- Register 117 (0x91) WHO_AM_I

12 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the ICG-20660.

Note: The device will come up in active mode upon power-up.

12.1 REGISTERS 0 TO 2 – GYROSCOPE SELF-TEST REGISTERS

Register Name: SELF_TEST_X_GYRO, SELF_TEST_Y_GYRO, SELF_TEST_Z_GYRO
Type: READ/WRITE
Register Address: 00, 01, 02 (Decimal); 00, 01, 02 (Hex)

REGISTER	BIT	NAME	FUNCTION
SELF_TEST_X_GYRO	[7:0]	XG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_GYRO	[7:0]	YG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_GYRO	[7:0]	ZG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round\left(\frac{\log(ST\_FAC/(2620/2^{FS}))}{\log(1.01)}\right) + 1$$

12.2 REGISTER 4 – GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: XG_OFFS_TC_H
Register Type: READ/WRITE
Register Address: 04 (Decimal); 04 (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved
[1:0]	XG_OFFS_TC_H[9:8]	Bits 9 and 8 of the 10-bit offset of X gyroscope (2's complement)

12.3 REGISTER 5 – GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: XG_OFFS_TC_L

Type: READ/WRITE

Register Address: 05 (Decimal); 05 (Hex)

BIT	NAME	FUNCTION
[7:0]	XG_OFFS_TC_L[7:0]]	Bits 7 to 0 of the 10-bit offset of X gyroscope (2's complement)

Description:

The temperature compensation (TC) registers are used to reduce gyro offset variation due to temperature change. The TC feature is always enabled. However the compensation only happens when a TC coefficient is programed during factory trim which gets loaded into these registers at power up or after a *DEVICE_RESET*. If these registers contain a value of zero, temperature compensation has no effect on the offset of the chip. The TC registers have a 10-bit magnitude and sign adjustment in all full scale modes with a resolution of 2.52 mdps/C steps.

If these registers contain a non-zero value after power up, the user may write zeros to them to see the offset values without TC with temperature variation. Note that doing so may result in offset values that exceed data sheet "Initial ZRO Tolerance" in other than normal ambient temperature (~25 °C). The TC coefficients maybe restored by the user with a power up or a *DEVICE_RESET*.

The above description also applies to registers 7-8 and 10-11.

12.4 REGISTER 07 – GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: YG_OFFS_TC_H

Register Type: READ/WRITE

Register Address: 07 (Decimal); 07 (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved
[1:0]	YG_OFFS_TC_H[9:8]	Bits 9 and 8 of the 10-bit offset of Y gyroscope (2's complement)

12.5 REGISTER 08 – GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: YG_OFFS_TC_L

Register Type: READ/WRITE

Register Address: 08 (Decimal); 08 (Hex)

BIT	NAME	FUNCTION
[7:0]	YG_OFFS_TC_L[7:0]]	Bits 7 to 0 of the 10-bit offset of Y gyroscope (2's complement)

12.6 REGISTER 10 – GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: ZG_OFFS_TC_H
Register Type: READ/WRITE
Register Address: 10 (Decimal); 0A (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved
[1:0]	ZG_OFFS_TC_H[9:8]	Bits 9 and 8 of the 10-bit offset of Z gyroscope (2's complement)

12.7 REGISTER 11 – GYROSCOPE OFFSET TEMPERATURE COMPENSATION (TC) REGISTER

Register Name: ZG_OFFS_TC_L
Register Type: READ/WRITE
Register Address: 11 (Decimal); 0B (Hex)

BIT	NAME	FUNCTION
[7:0]	ZG_OFFS_TC_L[7:0]]	Bits 7 to 0 of the 10-bit offset of Z gyroscope (2's complement)

12.8 REGISTERS 13 TO 15 – ACCELEROMETER SELF-TEST REGISTERS

Register Name: SELF_TEST_X_ACCEL, SELF_TEST_Y_ACCEL, SELF_TEST_Z_ACCEL
Type: READ/WRITE
Register Address: 13, 14, 15 (Decimal); 0D, 0E, 0F (Hex)

REGISTER	BITS	NAME	FUNCTION
SELF_TEST_X_ACCEL	[7:0]	XA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_ACCEL	[7:0]	YA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_ACCEL	[7:0]	ZA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (2620/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round\left(\frac{\log(ST\_FAC/(2620/2^{FS}))}{\log(1.01)}\right) + 1$$

12.9 REGISTERS 19 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: XG_OFFS_USRH
Register Type: READ/WRITE
Register Address: 19 (Decimal); 13 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

12.10 REGISTERS 20 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: XG_OFFS_USRL
Register Type: READ/WRITE
Register Address: 20 (Decimal); 14 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

12.11 REGISTERS 21 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: YG_OFFS_USRH
Register Type: READ/WRITE
Register Address: 21 (Decimal); 15 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

12.12 REGISTERS 22 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: YG_OFFS_USRL
Register Type: READ/WRITE
Register Address: 22 (Decimal); 16 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

12.13 REGISTERS 23 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: ZG_OFFS_USRH
Register Type: READ/WRITE
Register Address: 23 (Decimal); 17 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

12.14 REGISTER 24 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: ZG_OFFS_USRL
Register Type: READ/WRITE
Register Address: 24 (Decimal); 18 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register.

12.15 REGISTER 25 – SAMPLE RATE DIVIDER

Register Name: SMPLRT_DIV
Register Type: READ/WRITE
Register Address: 25 (Decimal); 19 (Hex)

BIT	NAME	FUNCTION
[7:0]	SMPLRT_DIV[7:0]	Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate. NOTE: This register is only effective when FCHOICE_B register bits are 2'b00, and (0 < DLPF_CFG < 7). This is the update rate of the sensor register: SAMPLE_RATE = INTERNAL_SAMPLE_RATE / (1 + SMPLRT_DIV) Where INTERNAL_SAMPLE_RATE = 1 kHz

12.16 REGISTER 26 – CONFIGURATION

Register Name: CONFIG
Register Type: READ/WRITE
Register Address: 26 (Decimal); 1A (Hex)

BIT	NAME	FUNCTION
[7]	-	Reserved.
[6]	FIFO_MODE	When set to '1', when the FIFO is full, additional writes will not be written to FIFO. When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.
[5:3]	EXT_SYNC_SET[2:0]	Enables the FSYNC pin data to be sampled. **EXT_SYNC_SET** / **FSYNC bit location** 0 – function disabled 1 – TEMP_OUT_L[0] 2 – GYRO_XOUT_L[0] 3 – GYRO_YOUT_L[0] 4 – GYRO_ZOUT_L[0] 5 – ACCEL_XOUT_L[0] 6 – ACCEL_YOUT_L[0] 7 – ACCEL_ZOUT_L[0] FSYNC will be latched to capture short strobes. This will be done such that if FSYNC toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe.
[2:0]	DLPF_CFG[2:0]	For the DLPF to be used, FCHOICE_B[1:0] is 2'b00. See the table below.

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below.

FCHOICE_B		DLPF_CFG	Gyroscope				Temperature Sensor
<1>	<0>		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)	Delay (ms)	3-dB BW (Hz)
X	1	X	8173	8595.1	32	0.064	4000
1	0	X	3281	3451.0	32	0.11	4000
0	0	0	250	306.6	8	0.97	4000
0	0	1	176	177.0	1	2.9	188
0	0	2	92	108.6	1	3.9	98
0	0	7	3281	3451.0	8	0.17	4000

12.17 REGISTER 27 – GYROSCOPE CONFIGURATION

Register Name: GYRO_CONFIG
Register Type: READ/WRITE
Register Address: 27 (Decimal); 1B (Hex)

BIT	NAME	FUNCTION
[7]	XG_ST	X Gyro self-test
[6]	YG_ST	Y Gyro self-test
[5]	ZG_ST	Z Gyro self-test
[4:3]	FS_SEL[1:0]	Gyro Full Scale Select: 00 = ±125 dps 01 = ±250 dps 10 = ±500 dps
[2]	-	Reserved
[1:0]	FCHOICE_B[1:0]	Used to bypass DLPF as shown in table 1 above.

12.18 REGISTER 28 – ACCELEROMETER CONFIGURATION

Register Name: ACCEL_CONFIG
Register Type: READ/WRITE
Register Address: 28 (Decimal); 1C (Hex)

BIT	NAME	FUNCTION
[7]	XA_ST	X Accel self-test
[6]	YA_ST	Y Accel self-test
[5]	ZA_ST	Z Accel self-test
[4:3]	ACCEL_FS_SEL[1:0]	Accel Full Scale Select: ±2g (00), ±4g (01), ±8g (10), ±16g (11)
[2:0]	-	Reserved

12.19 REGISTER 29 – ACCELEROMETER CONFIGURATION 2

Register Name: ACCEL_CONFIG2
Register Type: READ/WRITE
Register Address: 29 (Decimal); 1D (Hex)

BIT	NAME	FUNCTION
[7:6]	FIFO_SIZE[1:0]	Specifies FIFO size according to the following: 0 = 512 Bytes
[5:4]	DEC2_CFG[1:0]	Averaging filter settings for Low Power Accelerometer mode: 0 = Average 4 samples 1 = Average 8 samples 2 = Average 16 samples 3 = Average 32 samples
[3]	ACCEL_FCHOICE_B	Used to bypass DLPF as shown in the table below.
[2:0]	A_DLPF_CFG	Accelerometer low pass filter setting as shown in table 2 below.

Accelerometer Data Rates and Bandwidths (Low-Noise Mode)

ACCEL_FCHOICE_B	A_DLPF_CFG	Accelerometer		
		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)
1	X	1046.0	1100.0	4
0	0	218.1	235.0	1
0	1	218.1	235.0	1
0	2	99.0	121.3	1
0	3	44.8	61.5	1
0	4	21.2	31.0	1
0	5	10.2	15.5	1
0	6	5.1	7.8	1
0	7	420.0	441.6	1

The data output rate of the DLPF filter block can be further reduced by a factor of 1/(1+SMPLRT_DIV), where SMPLRT_DIV is an 8-bit integer. Following is a small subset of ODRs that are configurable for the accelerometer in the low-noise mode in this manner (Hz):

3.91, 7.81, 15.63, 31.25, 62.50, 125, 250, 500, 1K

The following table lists the approximate accelerometer filter bandwidths available in the low-power mode of operation for some example ODRs.

In the low-power mode of operation, the accelerometer is duty-cycled. The following table shows some example configurations for accelerometer low power mode.

Accelerometer Data Rates and Bandwidths (Low-Power Mode)

ACCEL_FCHOICE_B		1	0	0	0	0
A_DLPF_CFG		x	7	7	7	7
DEC2_CFG		x	0	1	2	3
Averages		1x	4x	8x	16x	32x
Ton (ms)		1.084	1.84	2.84	4.84	8.84
Noise BW (Hz)		1100.0	441.6	235.4	121.3	61.5
3-dB BW (Hz)		1046.0	420.0	218.0	110.0	55.3
SMPLRT_DIV	ODR (Hz)					
255	3.9	Valid	Valid	Valid	Valid	Valid
127	7.8	Valid	Valid	Valid	Valid	Valid
99	10.0	Valid	Valid	Valid	Valid	Valid
63	15.6	Valid	Valid	Valid	Valid	Valid
31	31.3	Valid	Valid	Valid	Valid	Valid
19	50.0	Valid	Valid	Valid	Valid	Valid
15	62.5	Valid	Valid	Valid	Valid	Valid
9	100.0	Valid	Valid	Valid	Valid	Valid
7	125.0	Valid	Valid	Valid	Valid	N/A
4	200.0	Valid	Valid	Valid	Valid	
3	250.0	Valid	Valid	Valid	N/A	
1	500.0	Valid	Valid	N/A		

12.20 REGISTER 30 – LOW POWER MODE CONFIGURATION

Register Name: LP_MODE_CFG
Register Type: READ/WRITE
Register Address: 30 (Decimal); 1E (Hex)

BIT	NAME	FUNCTION
[7:4]	-	Reserved
[3:0]	LPOSC_CLKSEL	Sets the frequency of waking up the chip to take a sample of accel data – the low power accel Output Data Rate

LPOSC_CLKSEL	Output Frequency (Hz)
0	0.24
1	0.49
2	0.98
3	1.95
4	3.91
5	7.81
6	15.63
7	31.25
8	62.50
9	125
10	250
11	500
12-15	Reserved

12.21 REGISTER 31 – WAKE-ON MOTION THRESHOLD (ACCELEROMETER)

Register Name: ACCEL_WOM_THR
Register Type: READ/WRITE
Register Address: 31 (Decimal); 1F (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_THR[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for accelerometer.

12.22 REGISTER 35 – FIFO ENABLE

Register Name: FIFO_EN
Register Type: READ/WRITE
Register Address: 35 (Decimal); 23 (Hex)

BIT	NAME	FUNCTION
[7]	TEMP_FIFO_EN	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – Function is disabled.
[6]	XG_FIFO_EN	1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – Function is disabled.
[5]	YG_FIFO_EN	1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – Function is disabled. Note: Enabling any one of the bits corresponding to the Gyros or Temp data paths, data is buffered into the FIFO even though that data path is not enabled.
[4]	ZG_FIFO_EN	1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – Function is disabled.
[3]	ACCEL_FIFO_EN	1 – Write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate. 0 – Function is disabled.
[2:0]	-	Reserved.

12.23 REGISTER 54 – FSYNC INTERRUPT STATUS

Register Name: FSYNC_INT
Register Type: READ to CLEAR
Register Address: 54 (Decimal); 36 (Hex)

BIT	NAME	FUNCTION
[7]	FSYNC_INT	This bit automatically sets to 1 when a FSYNC interrupt has been generated. The bit clears to 0 after the register has been read.

12.24 REGISTER 55 – INT PIN / BYPASS ENABLE CONFIGURATION

Register Name: INT_PIN_CFG
Register Type: READ/WRITE
Register Address: 55 (Decimal); 37 (Hex)

BIT	NAME	FUNCTION
[7]	INT_LEVEL	1 – The logic level for INT pin is active low. 0 – The logic level for INT pin is active high.
[6]	INT_OPEN	1 – INT pin is configured as open drain. 0 – INT pin is configured as push-pull.
[5]	LATCH_INT_EN	1 – INT pin level held until interrupt status is cleared. 0 – INT pin indicates interrupt pulse's width is 50us.
[4]	INT_RD_CLEAR	1 – Interrupt status is cleared if any read operation is performed. 0 – Interrupt status is cleared only by reading INT_STATUS register
[3]	FSYNC_INT_LEVEL	1 – The logic level for the FSYNC pin as an interrupt is active low. 0 – The logic level for the FSYNC pin as an interrupt is active high.
[2]	FSYNC_INT_MODE_EN	When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by F*SYNC_INT_LEVEL*. When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.
[1]	-	Reserved.
[0]	-	Reserved.

12.25 REGISTER 56 – INTERRUPT ENABLE

Register Name: INT_ENABLE
Register Type: READ/WRITE
Register Address: 56 (Decimal); 38 (Hex)

BIT	NAME	FUNCTION
[7:5]	WOM_EN	'111' – Enable WoM interrupt '000' – Disable WoM interrupt – This is the default setting.
[4]	FIFO_OFLOW_EN	1 – Enables a FIFO buffer overflow to generate an interrupt. 0 – Function is disabled.
[3]	-	Reserved.
[2]	-	Reserved.
[1]	-	Reserved.
[0]	DATA_RDY_INT_EN	Data ready interrupt enable.

12.26 REGISTER 58 – INTERRUPT STATUS

Register Name: INT_STATUS
Register Type: READ to CLEAR
Register Address: 58 (Decimal); 3A (Hex)

BIT	NAME	FUNCTION
[7]	WOM_X_INT	X-axis accelerometer WoM interrupt status. Cleared on Read.
[6]	WOM_Y_INT	Y-axis accelerometer WoM interrupt status. Cleared on Read.
[5]	WOM_Z_INT	Z-axis accelerometer WoM interrupt status. Cleared on Read.
[4]	FIFO_OFLOW_INT	This bit automatically sets to 1 when a FIFO buffer overflow has been generated. The bit clears to 0 after the register has been read.
[3]	-	Reserved.
[2]	-	Reserved.
[1]	-	Reserved.
[0]	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

12.27 REGISTERS 59 TO 64 – ACCELEROMETER MEASUREMENTS

Register Name: ACCEL_XOUT_H
Register Type: READ only
Register Address: 59 (Decimal); 3B (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_H[15:8]	High byte of accelerometer x-axis data.

Register Name: ACCEL_XOUT_L
Register Type: READ only
Register Address: 60 (Decimal); 3C (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_L[7:0]	Low byte of accelerometer x-axis data.

Register Name: ACCEL_YOUT_H
Register Type: READ only
Register Address: 61 (Decimal); 3D (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_H[15:8]	High byte of accelerometer y-axis data.

Register Name: ACCEL_YOUT_L
Register Type: READ only
Register Address: 62 (Decimal); 3E (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_L[7:0]	Low byte of accelerometer y-axis data.

Register Name: ACCEL_ZOUT_H
Register Type: READ only
Register Address: 63 (Decimal); 3F (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_H[15:8]	High byte of accelerometer z-axis data.

Register Name: ACCEL_ZOUT_L
Register Type: READ only
Register Address: 64 (Decimal); 40 (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_L[7:0]	Low byte of accelerometer z-axis data.

12.28 REGISTERS 65 AND 66 – TEMPERATURE MEASUREMENT

Register Name: TEMP_OUT_H
Register Type: READ only
Register Address: 65 (Decimal); 41 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[15:8]	High byte of the temperature sensor output.

Register Name: TEMP_OUT_L
Register Type: READ only
Register Address: 66 (Decimal); 42 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[7:0]	Low byte of the temperature sensor output. **TEMP_degC** = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 25degC

12.29 REGISTERS 67 TO 72 – GYROSCOPE MEASUREMENTS

Register Name: GYRO_XOUT_H
Register Type: READ only
Register Address: 67 (Decimal); 43 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[15:8]	High byte of the X-Axis gyroscope output.

Register Name: GYRO_XOUT_L
Register Type: READ only
Register Address: 68 (Decimal); 44 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[7:0]	Low byte of the X-Axis gyroscope output. **GYRO_XOUT =** Gyro_Sensitivity * X_angular_rate Nominal Conditions: FS_SEL = 0 Gyro_Sensitivity = 131 LSB/(º/s)

Register Name: GYRO_YOUT_H
Register Type: READ only
Register Address: 69 (Decimal); 45 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[15:8]	High byte of the Y-Axis gyroscope output.

Register Name: GYRO_YOUT_L
Register Type: READ only
Register Address: 70 (Decimal); 46 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[7:0]	Low byte of the Y-Axis gyroscope output. **GYRO_YOUT =** Gyro_Sensitivity * Y_angular_rate Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 131 LSB/(º/s)

Register Name: GYRO_ZOUT_H
Register Type: READ only
Register Address: 71 (Decimal); 47 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[15:8]	High byte of the Z-Axis gyroscope output

Register Name: GYRO_ZOUT_L
Register Type: READ only
Register Address: 72 (Decimal); 48 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[7:0]	Low byte of the Z-Axis gyroscope output. **GYRO_ZOUT =** Gyro_Sensitivity * Z_angular_rate Nominal FS_SEL = 0 Conditions Gyro_Sensitivity = 131 LSB/(º/s)

12.30 REGISTER 104 – SIGNAL PATH RESET

Register Name: SIGNAL_PATH_RESET
Register Type: READ/WRITE
Register Address: 104 (Decimal); 68 (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved.
[1]	ACCEL_RST	Reset accel digital signal path. Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.
[0]	TEMP_RST	Reset temp digital signal path. Note: Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.

12.31 REGISTER 105 – ACCELEROMETER INTELLIGENCE CONTROL

Register Name: ACCEL_INTEL_CTRL
Register Type: READ/WRITE
Register Address: 105 (Decimal); 69 (Hex)

BIT	NAME	FUNCTION
[7]	ACCEL_INTEL_EN	This bit enables the Wake-on-Motion detection logic.
[6]	ACCEL_INTEL_MODE	0 – Do not use. 1 – Compare the current sample with the previous sample.
[5:1]	-	Reserved
[0]	WOM_TH_MODE	0 – Set WoM interrupt on the OR of all enabled accelerometer thresholds. 1 – Set WoM interrupt on the AND of all enabled accelerometer thresholds. Default setting is 0.

12.32 REGISTER 106 – USER CONTROL

Register Name: USER_CTRL
Register Type: READ/WRITE
Register Address: 106 (Decimal); 6A (Hex)

BIT	NAME	FUNCTION
[7]	-	Reserved.
[6]	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface. To disable FIFO writes by DMA, use FIFO_EN register. -
[5]	-	Reserved
[4]	I2C_IF_DIS	1 – Reset I^2C Slave module and put the serial interface in SPI mode only. This bit auto clears after one clock cycle of the internal 20 MHz clock.
[3]	-	Reserved.
[2]	FIFO_RST	1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock.
[1]	-	Reserved.
[0]	SIG_COND_RST	1 – Reset all gyro digital signal path, accel digital signal path, and temp digital signal path. This bit also clears all the sensor registers.

12.33 REGISTER 107 – POWER MANAGEMENT 1

Register Name: PWR_MGMT_1
Register Type: READ/WRITE
Register Address: 107 (Decimal); 6B (Hex)

BIT	NAME	FUNCTION
[7]	DEVICE_RESET	1 – Reset the internal registers and restores the default settings. The bit automatically clears to 0 once the reset is done.
[6]	SLEEP	When set to 1, the chip is set to sleep mode.
[5]	CYCLE	When set to 1, and SLEEP and STANDBY are not set to 1, the chip will cycle between sleep and taking a single accelerometer sample at a rate determined by SMPLRT_DIV. **Note:** When all accelerometer axes are disabled via PWR_MGMT_2 register bits and cycle is enabled, the chip will wake up at the rate determined by the respective registers above, but will not take any samples.
[4]	GYRO_STANDBY	When set, the gyro drive and pll circuitry are enabled, but the sense paths are disabled. This is a low power mode that allows quick enabling of the gyros.
[3]	TEMP_DIS	When set to 1, this bit disables the temperature sensor.
[2:0]	CLKSEL[2:0]	**Code** **Clock Source** 0 Internal 20 MHz oscillator 1 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 2 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 3 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 4 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 5 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 6 Internal 20 MHz oscillator 7 Stops the clock and keeps timing generator in reset

Note: The default value of CLKSEL[2:0] is 000. It is required that CLKSEL[2:0] be set to 001 to achieve full gyroscope performance.

12.34 REGISTER 108 – POWER MANAGEMENT 2

Register Name: PWR_MGMT_2
Register Type: READ/WRITE
Register Address: 108 (Decimal); 6C (Hex)

BIT	NAME	FUNCTION
[7]	**[7]**	FIFO_LP_EN
[6]	-	Reserved.
[5]	STBY_XA	1 – X accelerometer is disabled. 0 – X accelerometer is on.
[4]	STBY_YA	1 – Y accelerometer is disabled. 0 – Y accelerometer is on.
[3]	STBY_ZA	1 – Z accelerometer is disabled. 0 – Z accelerometer is on.
[2]	STBY_XG	1 – X gyro is disabled. 0 – X gyro is on.
[1]	STBY_YG	1 – Y gyro is disabled. 0 – Y gyro is on.
[0]	STBY_ZG	1 – Z gyro is disabled. 0 – Z gyro is on.

12.35 REGISTER 114 AND 115 – FIFO COUNT REGISTERS

Register Name: FIFO_COUNTH
Register Type: READ Only
Register Address: 114 (Decimal); 72 (Hex)

BIT	NAME	FUNCTION
[7:5]	-	Reserved.
[4:0]	FIFO_COUNT[12:8]	High Bits, count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

Register Name: FIFO_COUNTL
Register Type: READ Only
Register Address: 115 (Decimal); 73 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_COUNT[7:0]	Low Bits, count indicates the number of written bytes in the FIFO. NOTE: Must read FIFO_COUNTH to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

12.36 REGISTER 116 – FIFO READ WRITE

Register Name: FIFO_R_W
Register Type: READ/WRITE
Register Address: 116 (Decimal); 74 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_DATA[7:0]	Read/Write command provides Read or Write operation for the FIFO.

Description:

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 59 through 72 will be written in order at the Sample Rate.

The contents of the sensor data registers (Registers 59 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0xFF until new data is available. Normal data is precluded from ever indicating 0xFF, so 0xFF gives a trustworthy indication of FIFO empty.

12.37 REGISTER 117 – WHO AM I

Register Name:
Register Type: READ only
Register Address: 117 (Decimal); 75 (Hex)

BIT	NAME	FUNCTION
[7:0]	WHO_AM_I	Register to indicate to user which device is being accessed.

This register is used to verify the identity of the device. The contents of *WHO_AM_I* is an 8-bit device ID. The default value of the register is 0x91. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor. The I^2C address of the ICG-20660 is 0x68 or 0x69 depending upon the value driven on AD0 pin.

12.38 REGISTERS 119, 120, 122, 123, 125, 126 ACCELEROMETER OFFSET REGISTERS

Register Name: XA_OFFSET_H
Register Type: READ/WRITE
Register Address: 119 (Decimal); 77 (Hex)

BIT	NAME	FUNCTION
[7:0]	XA_OFFS[14:7]	Upper bits of the X accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps.

Register Name: XA_OFFSET_L
Register Type: READ/WRITE
Register Address: 120 (Decimal); 78 (Hex)

BIT	NAME	FUNCTION
[7:1]	XA_OFFS[6:0]	Lower bits of the X accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved.

Register Name: YA_OFFSET_H
Register Type: READ/WRITE
Register Address: 122 (Decimal); 7A (Hex)

BIT	NAME	FUNCTION
[7:0]	YA_OFFS[14:7]	Upper bits of the Y accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps.

Register Name: YA_OFFSET_L
Register Type: READ/WRITE
Register Address: 123 (Decimal); 7B (Hex)

BIT	NAME	FUNCTION
[7:1]	YA_OFFS[6:0]	Lower bits of the Y accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved.

Register Name: ZA_OFFSET_H
Register Type: READ/WRITE
Register Address: 125 (Decimal); 7D (Hex)

BIT	NAME	FUNCTION
[7:0]	ZA_OFFS[14:7]	Upper bits of the Z accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps.

Register Name: ZA_OFFSET_L
Register Type: READ/WRITE
Register Address: 126 (Decimal); 7E (Hex)

BIT	NAME	FUNCTION
[7:1]	ZA_OFFS[6:0]	Lower bits of the Z accelerometer offset cancellation. +/- 16g Offset cancellation in all Full Scale modes, 15 bit 0.98-mg steps.
[0]	-	Reserved.

13 REVISION HISTORY

Revision Date	Revision	Description
05/27/2016	1.0	Initial Draft
09/20/2016	1.1	Removed preliminary, formatting updates
03/18/2021	1.2	Added Note on page 17; Added Sections 4.18 and 4.19

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