| PCN Number: | 20151207004 | PCN Date: | 12/10/2015 |
|---|---|---|---|
| Title: | Qualification of Aizu as an additional wafer fab site option for select CMOS9T devices | | |
| Customer Contact: | PCN Manager | Dept: | Quality Services |
| Proposed 1st Ship Date: | 03/10/2016 | Estimated Sample Availability: | Date provided at sample request. |

| Change Type: | | | | | |
|---|---|---|---|---|---|
| ☐ | Assembly Site | ☐ | Assembly Process | ☐ | Assembly Materials |
| ☐ | Design | ☐ | Electrical Specification | ☐ | Mechanical Specification |
| ☐ | Test Site | ☐ | Packing/Shipping/Labeling | ☐ | Test Process |
| ☐ | Wafer Bump Site | ☐ | Wafer Bump Material | ☐ | Wafer Bump Process |
| ☒ | Wafer Fab Site | ☐ | Wafer Fab Materials | ☐ | Wafer Fab Process |
| | | ☐ | Part number change | | |

## PCN Details

**Description of Change:**

This change notification is to announce the qualification of Aizu as an additional wafer fab site option for the CMOS9T devices listed in the product affected section of this document.

| Current | | | Additional | | |
|---|---|---|---|---|---|
| **Current Fab Site** | **Process** | **Wafer Diameter** | **Additional Fab Site** | **Process** | **Wafer Diameter** |
| Maine Fab | CMOS9T | 200 mm | **Aizu** | **CMOS9T** | **200 mm** |

The CMOS9T process technology was qualified at MFAB in January 2015. Qualification details are shown in the Qual Data Section of this document.

**Reason for Change:**

Continuity of Supply

**Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):**

None

**Changes to product identification resulting from this PCN:**

**Current**

| Chip Sites | Chip Site Origin Code (20L) | Chip Site Country Code (21L) | Chip Site City |
|---|---|---|---|
| Maine Fab | CUA | USA | South Portland |

**New**

| Chip Site | Chip Site Origin Code (20L) | Chip Site Country Code (21L) | Chip Site City |
|---|---|---|---|
| **Aizu** | **CU2** | **JPN** | Aizuwakamatsu-shi |

Sample product shipping label (not actual product label)

| Product Affected: | | | |
|---|---|---|---|
| FDC1004DGSR | LDC1041NHRR | LDC1312DNTT | LDC1614RGHT |
| FDC1004DGST | LDC1041NHRT | LDC1314RGHR | TPL5010DDCR |
| FDC1004DSCJ | LDC1051NHRJ | LDC1314RGHT | TPL5010DDCT |
| FDC1004DSCR | LDC1051NHRR | LDC1612DNTR | TPL5110DDCR |
| FDC1004DSCT | LDC1051NHRT | LDC1612DNTT | TPL5110DDCT |
| LDC1041NHRJ | LDC1312DNTR | LDC1614RGHR | |

# Qualification Report

## CMOS9T DGO Process at Aizu
## Approved 01/11/2015

### Die Attributes

| Attributes | Qual Device : LP8754YFQ | QBS Process: LM3533TMX-40/NOPB | QBS Process: LP8556TMX-E09/S1 | QBS Process: LP5907UVX-3.3 |
|---|---|---|---|---|
| Wafer Fab Site | Aizu | Aizu | Aizu | Aizu |
| Wafer Fab Process | CMOS9T | CMOS9T | CMOS9T | CMOS9T |
| Wafer Diameter | 200mm | 200mm | 200mm | 200mm |

- QBS: Qual By Similarity
- Qual Device LP8754YFQ is qualified at LEVEL1-260C
- Qual Device LP8754YFQ CONTROL is qualified at LEVEL1-260C

### Qualification Results
### Data Displayed as: Number of lots / Total sample size / Total failed

| Type | Test Name / Condition | Duration | Qual Device : LP8754YFQ | QBS Process: LM3533TMX-40/NOPB | QBS Process: LP8556TMX-E09/S1 | QBS Process: LP5907UVX-3.3 |
|---|---|---|---|---|---|---|
| PC | PreCon Level 1 | 260C | - | 3/462/0 | 3/693/0 | 3/693/0 |
| HAST | Biased HAST, 110C/85%RH | 264 Hours | - | - | 2/154/0 | - |
| AC | Autoclave 121C | 96 hours | - | 3/231/0 | - | - |
| THB | Biased Temperature and Humidity, 85C/85%RH | 1000 Hours | - | - | - | 3/231/0 |
| UHAST | Unbiased HAST 130C/85%RH | 96 Hours | - | - | 3/231/0 | 3/231/0 |
| TC | Temperature Cycle, -65/150C | 500 Cycles | - | 3/231/0 | 3/231/0 | 3/231/0 |
| HTSL | High Temp Storage Bake 150C | 500/hrs - 150C | - | - | 1/77/0 | - |
| HTOL | Life Test, 125C | 1000 Hours | 3/231/0 | - | - | - |

| | | | | | | |
|---|---|---|---|---|---|---|
| ELFR | Early Life Failure Rate, 125C | 48 Hours | 3/2449/0 | - | - | - |
| HBM | ESD - HBM | 1000 V | 3/9/2000 | - | - | - |
| CDM | ESD - CDM | 750 V | 3/9/2000 | - | - | - |
| LU | Latch-up | 25 C | 3/18/2000 | - | - | - |
| LU | Latch-up | 125 C | 3/18/2000 | - | - | - |
| ED | Electrical Characterization | - | 3/90/0 | - | | - |
| DR | Data Retention, 215C | 300 Hours | 3/231/0 | - | - | - |
| PC | EPROM Power Cycles (on/off) | 10,000 Cycles | 3/231/0 | - | - | - |
| WLR | Wafer level Reliability | Per Site Specification | pass | - | - | - |

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

**Green/Pb-free Status:**

Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

| Location | E-Mail |
|---|---|
| USA | PCNAmericasContact@list.ti.com |
| Europe | PCNEuropeContact@list.ti.com |
| Asia Pacific | PCNAsiaContact@list.ti.com |
| Japan | PCNJapanContact@list.ti.com |