Datasheet Brief

MCDP2900

DisplayPort1.4a to HDMI2.0b Protocol Converter with HDCP2.3 Repeater

Features

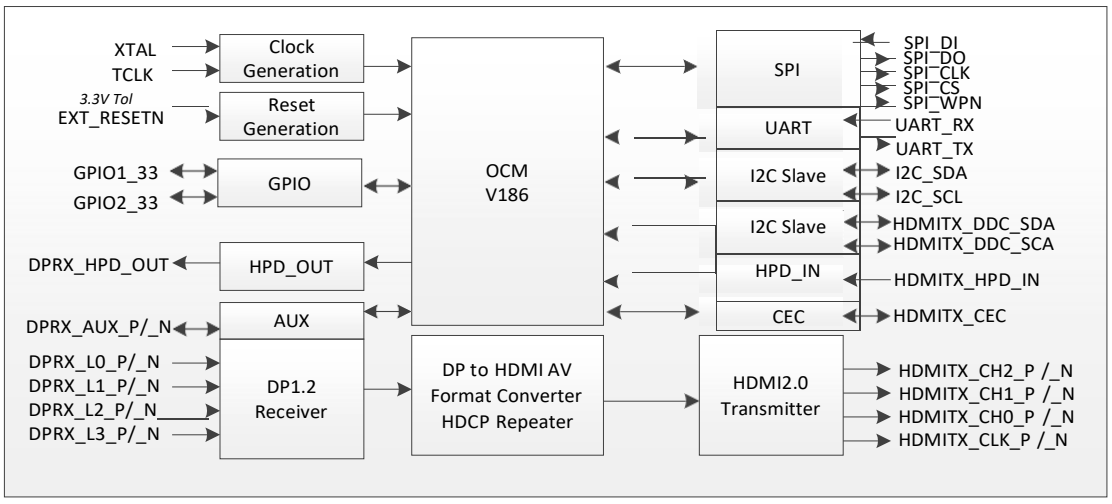
- DisplayPort™ (DP) ver. 1.4a Link layer receiver
  - Up to 5.4Gbps Link rate supporting HBR2/HBR/RBR modes
  - 1, 2, or 4 lanes configuration
  - Programmable receiver equalization
  - Single Stream
  - AUX CH 1 Mbps
  - 3.3V HPD_OUT
  - Link Training (LT) enhancements as in DP1.4a specification
  - Supports eDP ASSR scrambler operation
  - Video Stream Handling
    - Up to 600MHz dual pixel path and 16bpc
    - RGB/ YCbCr 444/422/420 pixel format
    - Horizontal expansion of VESA CVT to CEA timings as per DP1.4a specification
  - DPCD and CEC
    - Supports DPCD data structure revision 1.4 as per DP1.4a specification
    - Supports CEC tunneling over AUX
  - DP to HDMI Stereoscopic 3D Transport
    - Frame Sequential to Stacked Top-Bottom Conversion
    - Pass-through of other 3D formats
  - Audio Stream handling
    - LPCM and Compressed Audio encoding formats
    - Max Audio sample rate of 192KHz x8 Channel or 768KHz x2 Channel
- HDMI ver. 2.0b transmitter
  - 600 MHz maximum TMDS character clock
  - DC-coupled outputs with source termination
  - TMDS character-clock divide_by_4 Mode
  - Scrambling over HDMI2.0b
  - Programmable edge rate control
  - Programmable pre-emphasis control
  - Deep color up to 16 bits per color
  - High Dynamic Range support (Static and Dynamic HDR)
  - 3D video timings
  - CEC support – snooping, tunneling
  - HPD_IN handling
  - SCDC read request handling
    - Polling enabled for HDMI sinks not supporting read requests
- Video Input Processing (up to 6Gbps)
  - Color space conversion
  - 10 bits per color input width
  - 12 bits per color output width
  - 16 bits per color pass through
  - Programmable coefficient 3x3 matrix
  - Programmable input offset
  - Programmable output offset
  - Programmable output clipping levels
- Chroma Down Sampling
  - 5-tap H & V FIR filters with programmable coefficients
  - 12 bits per color input width
  - 12 bits per color output width
  - YCbCr444 to YCbCr420 conversion
  - YCbCr444 to YCbCr422 conversion
  - YCbCr422 to YCbCr420 conversion
  - Bypass chroma down-sampling for YCbCr420 input over DP Link
- Max video resolution and color depth on HDMI TX output
  - 4Kp60Hz, RGB/YCbCr444, 8 bpc
  - 4Kp60Hz, YCbCr422 up to 12 bpc
  - 4Kp60Hz, YCbCr420, up to 16 bpc
  - 4Kp30Hz, RGB/YCbCr444, up to 16 bpc
- Audio stream forwarding from DP RX to HDMI TX
  - Up to 8-ch, 192 kHz, 24 bps LPCM audio, AC3, DTS, Dolby-HD
  - 2-ch, 768 kHz 24 bps HBR audio
- HDCP support

  - HDCP1.3 to HDCP1.4 Repeater function
  - HDCP2.3 to HDCP1.4 Repeater function
  - HDCP2.3 to HDCP2.3 Repeater function
  - Read-protected embedded HDCP keys
- Enhanced security
  - Encrypted on-chip key storage
  - Security signed application firmware
  - Secure boot-up procedure
  - Debug ports disabled in production
- Metadata handling
  - HDMI TX DVI/HDMI mode setting (DPCD register)
  - YCbCr444-420 conversion (DPCD register)
  - IEC60958 BYTE3 Channel Status overwrite
  - CEA861F INFOFRAME generation
  - CEA861.3 HDR and Mastering InfoFrame as per DP1.4a specification
- Device configuration options
  - 8Mbit SPI flash for firmware binary image storage
  - AUX CH, I2C host interface
- Internal video pattern generator
  - Configurable through DPCD registers
- EMI reduction support
  - Spread spectrum for DP input
  - Scrambler for DP input and HDMI output
- Low power operation
  - 570 mW in protocol converter operation
  - 11 mW sleep mode operation
- ESD specification
  - ESD: +/-2 KV HBM, 500 V CDM
  - ESD: +/-6.5 KV HBM connector facing pins
- Package
  - 64 LFBGA (7 x 7 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Notebook, Tablet Accessories (USB Type-C dongles, docking stations)
- TV, Signage, Game consoles, STB

Figure 1. MCDP2900 block diagram



1. Description

The MCDP2900 is a power-optimized DisplayPort1.4a-to-HDMI2.0b converter, targeted for enabling USB Type-C DP Alt mode on TVs, Game consoles and other consumer equipment as well as for mobile PC and tablet accessory applications. This device functions as an active protocol converter with HDCP1.x/ HDCP2.3 repeater supporting HDR video quality for deep color media content playback.

MCDP2900 behaves as a DP branch device with a DP-to-HDMI transport protocol converter function and allows a DP or USB Type-C source to drive an HDMI sink device. The maximum TMDS character clock frequency supported is 600 Mchar/s (per HDMI2.0b specification).

The MCDP2900 operates with two power supply voltages: 1.2 V and 3.3 V. It consumes:

- 570 mW in protocol converter operation
- 11 mW sleep mode operation

The MCDP2900 has a DP1.4a receiver and an HDMI2.0b transmitter. The DP receiver supports up to 5.4Gbps/lane over 4 lanes. It supports DP SST transport format on its main link and Manchester-coded AUX signaling as the side band channel. The downstream HDMI TX port is HDMI2.0b specification compliant.

The MCDP2900 is capable of supporting Ultra High-Definition video formats with resolutions as high as 4096 x 2160 progressive @ 60 Hz (4K2Kp60Hz). It supports RGB/YCbCr video color formats with a color depth of 16 bpc (bits per component or 48 bits per pixel) as long as it fits within the DP and HDMI link bandwidth. This device also supports pixel encoding conversion from RGB or YCbCr444 to YCbCr420 and a YcbCr420 pass- through function. In addition, High Dynamic Range (HDR) with deep color up to 12bpc at 4Kp60Hz is supported through the conversion of RGB/YCbCr444 over DP link to YCbCr420 on the HDMI output with a horizontal expansion to CEA timings.

This device offers secure reception and transmission of high bandwidth digital audio and video content with HDCP1.3 and HDCP2.3 content protection for the upstream DP interface. It also supports HDCP1.4 and HDCP2.3 repeater function compliant to the latest CTS specification.

The MCDP2900 uses an external crystal of 27 MHz as a reference clock for its operation. An internal Power On Reset (POR) circuit senses the voltage on the reset input and provides the chip reset during system power-up. The device has an internal microcontroller with SPI, UART (debug only), and I2C system interface signals. It uses an external 8Mbit SPI flash memory for storing a secure signed firmware image with fail-safe recovery. Firmware update to the SPI flash is done securely through the DP AUX_CH or the I2C host interface. The secure programming (In-System-Programming), secure boot and application FW signing process uses RSA 2048-bit root and leaf public/private key pairs.

2. Application overview

The target applications of MCDP2900 are the notebook, tablet accessories i.e., adaptors (dongles), docking stations and other AV accessories. MCDP2900 is also intended for enabling USB Type-C DP alternative mode for inside-the-box applications such as TVs, game consoles and other consumer equipment.

3. Ordering information

Table 1. Order codes

Part Number	Operating Temperature	Package
MCDP2900A4	0°C to +70°C	64 LFBGA (7x7x1.4 mm) in Tray
MCDP2900A4T	0°C to +70°C	64 LFBGA (7x7x1.4 mm) in Tape & Reel