PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8289
Dated 05 Feb 2014

STLUX385A Metal mask change

Table 1. Change Implementation Schedule

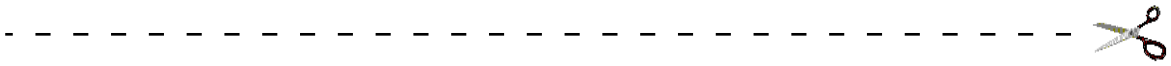
Forecasted implementation date for change	29-Jan-2014
Forecasted availability date of samples for customer	29-Jan-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	29-Jan-2014
Estimated date of changed product first shipment	07-May-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	STLUX385A and STLUX385ATR
Type of change	Product design change
Reason for change	To improve the IC robustness during initialization at start-up
Description of the change	We have introduced a minor modification through a metal mask change on product line F125 upgrading from AEG to AFG revision.
Change Product Identification	By a new internal part number (Finished Goods code)
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8289**
Please sign and return to STMicroelectronics Sales Office	**Dated 05 Feb 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Vavassori, Emanuele	Marketing Manager
Vavassori, Emanuele	Product Manager
Moretti, Paolo	Q.A. Manager

ATTACHMENT TO PCN IPG-IPC/13/8289

WHAT*:*
We have introduced a minor modification through a metal mask change on product line F125, upgrading from AEG to AFG revision.

The impacted products are :

Product Line	Package description	Commercial Product	Packing Type
F125	TSSOP 38	STLUX385A	Tube
		STLUX385ATR	Tape & Reel

WHY*:*
During the IC start-up phase, in specific process/temperature/application conditions, the reset procedure was not completely effective.
As a consequence, a few pins of the IC were not working as expected, behaving as per one of the manufacturing test mode configurations.
This situation persisted until a new and effective start-up phase happened.

HOW*:*
Through a metal mask modification.
The changed product will be identified by a new Finished Goods code.

WHEN*:*
The metal mask change has been already implemented and evaluated (see attached Reliability Report RR000114CS6080).
A detailed technical report can be provided on request.

Samples of the new revision are available.

Reliability Report

General Information	
Product Line	*F125*
Product Description	*Low Power 8-bit Microcontroller*
Product division	*I&PC*
Package	*TSSOP38*
Silicon process technology	*CMOSF9*

Locations	
Wafer fab location	*ROUSSET*
Assembly plant location	*AMKOR ATP1 PHILIPPINES*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	16-Jan-14	11	G. D'Angelo	Original document

Issued by

Gianfranco D'Angelo

Approved by

Alceo Paratore

Table of Contents

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation performed on the F125 device diffused in ROUSSET and assembled in TSSOP38 in AMKOR ATP1 PHILIPPINES.

Below the list of the trials scheduled on the Reliability Qualification Plan:

Die Oriented Tests

- High Temperature Operating Life (H.T.O.L.)
- Data Retention bake after Programming (D.R.B)

Package Oriented Tests

- Preconditioning (Prec.)
- Temperature Cycling (T.C.)
- Autoclave (A.C.)
- High Temperature Storage Life (H.T.S.L.)

Electrical Characterization

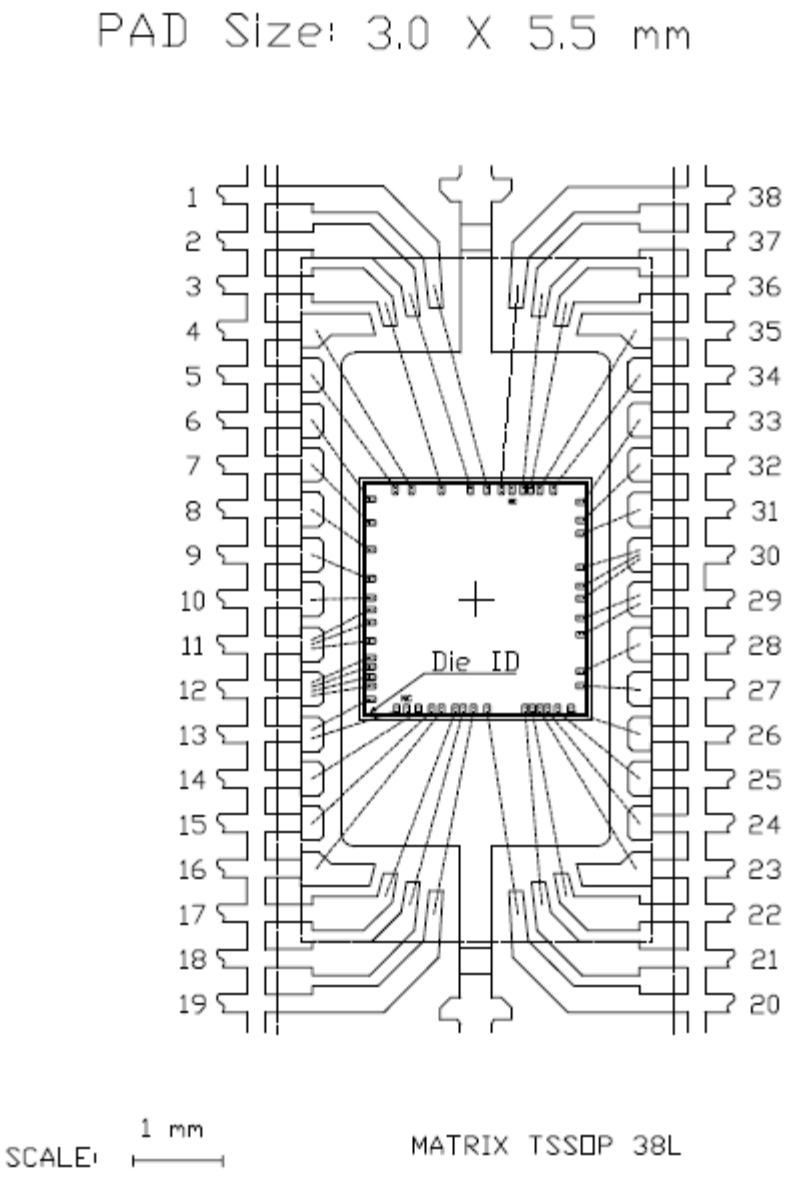
- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the trials performed on **the F125 device diffused in ROUSSET and assembled in TSSOP38 in AMKOR ATP1 PHILIPPINES can be qualified from reliability viewpoint**

3 DEVICE CHARACTERISTICS

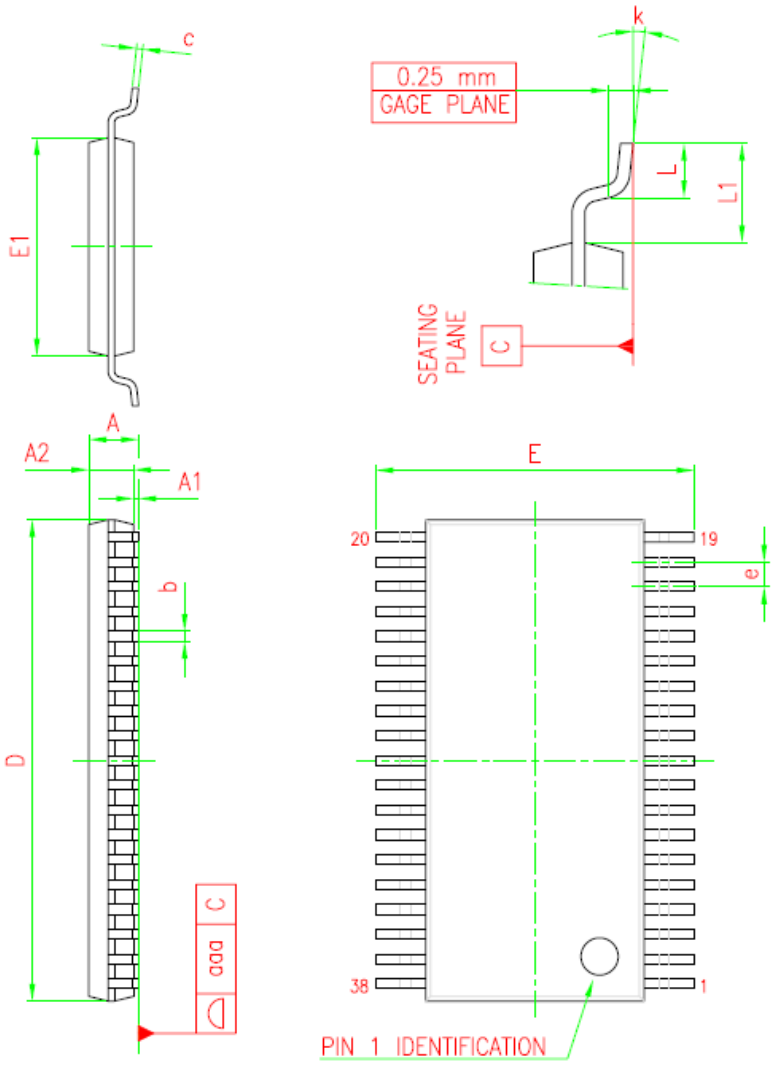
3.1 Bonding diagram



3.2 Package outline/Mechanical data

	DIMENSIONS						
	DATABOOK (mm)			DRAWING (mm)			
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	NOTES
A			1.20	0.925	1.00	1.075	
A1	0.05		0.15	0.065	0.10	0.135	
A2	0.80	1.00	1.05	0.86	0.90	0.94	
b	0.17		0.27			0.255	
c	0.09		0.20			0.165	
D	9.60	9.70	9.80	9.77	9.70	9.73	(2)
E	6.20	6.40	6.60	6.30	6.40	6.50	
E1	4.30	4.40	4.50	4.37	4.40	4.43	(3)
e		0.50		0.45	0.50	0.55	
L	0.45	0.60	0.75	0.525	0.60	0.675	
L1		1.00			1.00		
k	0		8	2	4	6	DEGREES
aaa			0.10			0.06	

FIGURE.1 : TSSOP 38L BODY 4.40mm LEAD PITCH 0.50mm
PACKAGE CODE : YK



Device Characteristics

3.3 Traceability

Wafer fab information	
Wafer fab manufacturing location	*ROUSSET*
Wafer diameter	*8 inches*
Wafer thickness	*280µm*
Silicon process technology	*CMOSF9*
Die finishing back side	*Lapped Silicon*
Bond pad metallization layers	*Cu*
Passivation	*USG+SiN*
Metal levels	*4*

Assembly Information	
Assembly plant location	*AMKOR ATP1 PHILIPPINES*
Package description	*TSSOP38*
Molding compound	*Sumitomo G700K*
Wires bonding materials/diameters	*Au/1.0 mils*
Die attach material	*Ablestick 8290*
Lead solder material	*Pure Tin*

4 TESTS RESULTS SUMMARY

4.1 Test plan and results summary

Test	Method	Conditions	Failure/SS Lot 1	Lot 2	Lot 3	Duration	Note
Die Oriented Tests (performed on AXG revision)							
HTOL	High Temperature Operating Life						
	PC before	**Tj=150°C** ***Vdd=5.5v, with SCAN, BIST and Funcional pattern and switch ON/OFF cycles***	**0/77**	**-**	**-**	**2488h (*)**	
DRB	Data Retention bake after Programming						
		Tamb=150°C ***EEprom programmed at time 0h (CHARGE)***	**0/77**	**-**	**-**	**4130h**	
Die Oriented Tests (performed on AEG revision)							
DRB	Data Retention bake after Programming						
		Tamb=175°C ***EEprom programmed at time 0h (CHARGE)***	**0/77**	**-**	**-**	**1643h**	
Package Oriented Tests (performed on AXG revision)							
PC	Preconditioning JL3						
		Tpeak=260°C, 24h bake@125°C, 195h@30°C/60%RH, 3 reflow	**0/231**	**-**	**-**		
AC	Autoclave						
	PC Before	**121°C 2atm**	**0/77**	**-**	**-**	**168h**	
TC	Temperature Cycling						
	PC Before	**-50°C/150°C in air**	**0/77**	**-**	**-**	**1000cy**	
Electrical Characterization Tests (performed on AXG revision)							
ESD	Electro Static Discharge						
	Human Body Model	**+/- 2kV**	**0/3**	**-**	**-**		
	Machine Model	**+/- 200V**	**0/3**				
	Charge Device Model	**+/- 1kV**	**0/3**				
LU	Latch-Up						
	Over-voltage and Current Injection	**Tamb=105°C** **Jedec78 – Level B**	**0/6**	**-**	**-**		
Electrical Characterization Tests (performed on AEG revision)							
ESD	Electro Static Discharge						
	Charge device Model	**+/- 750V**	**0/3**	**-**	**-**		

(*) 2488h have been performed as characterization purpose
Note: the F125 AFG rev. is a metal option of the previous revisions and from reliability point of view and can be qualified by similarity.

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168hrs, 500hrs, 1000hrs, 1650hrs, 2000hrs @ Ta=25°C
- Final Testing (2488 hrs) @ Ta=25°C

5.1.2 Data Retention bake after Programming

The device is submitted to high temperature storage with all cells programmed (All0 pattern) in its EEPROM memory to investigate data retention properties of memory cells.

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5.2 Package oriented tests

5.2.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.
The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "popcorn" effect and delamination

5.2.2 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.3 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

5.3 Electrical Characterization Tests

5.3.1 Latch-Up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-100mA	Inom+100mA	V5.5=8.1V
IN high: 5.5V	-100mA	Inom+100mA	V5.5=8.1V

5.3.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** JEDEC STANDARD JESD22-A114
  DCF-AEC-Q100-002
- **Machine Model** JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** ANSI/ESD STM 5.3.1 ESDA
  CDF-AEC-Q100-011

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